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SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Jan W1
         (c) 2002 Institution of Electrical Engineers
  File   6:NTIS  1964-2002/Jan W3
         (c) 2002 NTIS, Intl Cpyrght All Rights Res
*File   6: See HELP CODES6 for a short list of the Subject Heading Codes
(SC=, SH=) used in NTIS.
  File   8:Ei Compendex(R)  1970-2002/Jan W1
         (c) 2002 Engineering Info. Inc.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Jan W1
         (c) 2002 Inst for Sci Info
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2001/Dec
         (c) 2001 ProQuest Info&Learning
  File  77:Conference Papers Index  1973-2001/Nov
         (c) 2001 Cambridge Sci Abs
  File  94:JICST-EPlus  1985-2002/Nov W4
         (c)2002 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2001/Nov
         (c) 2001 The HW Wilson Co.
  File 108:AEROSPACE DATABASE  1962-2001/DEC
         (c) 2001 AIAA
*File 108: For update information please see Help News108.
  File 144:Pascal  1973-2002/Dec W5
         (c) 2002 INIST/CNRS
  File 238:Abs. in New Tech & Eng.  1981-2001/Dec
         (c) 2001 Reed-Elsevier (UK) Ltd.
  File 305:Analytical Abstracts  1980-2002/Dec W5
         (c) 2002 Royal Soc Chemistry
*File 305: Frequency of updates and Alerts changing to weekly.
See HELP NEWS 305.
  File 315:ChemEng & Biotec Abs  1970-2001/Oct
         (c) 2001 DECHEMA
  File  14:Mechanical Engineering Abs  1973-2002/Jan
         (c) 2002 Cambridge Sci Abs
  File  65:Inside Conferences  1993-2002/Jan W1
         (c) 2002 BLDSC all rts. reserv.
*File  65: For variance in UDs please see Help News65.
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Set     Items   Description
S1          2   AU="CARL RJ"
S2         33   AU="CARL, R." OR AU="CARL, R. J." OR AU="CARL, R. J., JR."
                OR E10-E11
S3         12   AU="CARL R" OR AU="CARL RJ"
S4          1   AU="AXEL B"
S5         46   S1:S4
S6       1260   (ANTI(W)FUSE? ?) OR ANTIFUSE? ? OR OTP OR ((ONE)(N)(TIME)(
                N)(PROGRAM?))
S7     375051   (DIELECTRIC? OR OXIDE OR INSULAT?)(3N)(FILM? ? OR LAYER? OR
                COAT???? OR MATERIAL?)
S8          0   S5 AND S6
S9         13   S5 AND S7
? RD

...completed examining records
     S10       7  RD (unique items)
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? T S10/3,AB/1-7

>>>No matching display code(s) found in file(s): 65

10/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6131228 INSPEC Abstract Number: A1999-04-8115H-012, B1999-02-0520F-057
Title: Common and unique aspects of perovskite thin film CVD processes
Author(s): Van Buskirk, P.C.; Roeder, J.F.; Baum, T.H.; Bilodeau, S.M.; Russell, M.W.; Johnston, S.T.; **Carl, R.J.**; Desrochers, D.J.; Hendrix, B.C.; Hintermaier, F.
Author Affiliation: ATMI Inc., Danbury, CT, USA
Journal: Integrated Ferroelectrics Conference Title: Integr. Ferroelectr. (Netherlands) vol.21, no.1-4 p.273-89
Publisher: Gordon & Breach,
Publication Date: 1998 Country of Publication: Netherlands
CODEN: IFEREU ISSN: 1058-4587
SICI: 1058-4587(1998)21:1/4L.273:CUAP;1-V
Material Identity Number: G361-1998-003
Conference Title: 10th International Symposium on Integrated Ferroelectrics
Conference Date: 1-4 March 1998 Conference Location: Monterey, CA, USA
Language: English
Abstract: In the past 5 years there has been a large amount of work to develop CVD technology for the deposition of the predominant perovskite **oxide** thin **films**, (Ba,Sr)TiO/sub 3/, SrBi/sub 2/Ta/sub 2/O/sub 9/ and Pb(Zr,Ti)O/sub 3/. For each of these families of materials, CVD processes have matured such that state-of-the-art film properties may be achieved with this technique. Much of the progress is attributed to the use of the liquid delivery technique to transfer relatively involatile metalorganic precursors to the reactor. This paper discusses common attributes of these thermal CVD processes, particularly the precursors, delivery methodology and reactor hardware. The paper also highlights unique aspects that differentiate the processes, including the CVD decomposition regime, strategies for film composition control and approaches for forming the crystalline perovskite phase. Representative film properties are presented, demonstrating that these processes are becoming increasingly mature.
Subfile: A B

10/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5730579 INSPEC Abstract Number: B9712-2810-001
Title: Resistance degradation of CVD (Ba,Sr)TiO/sub 3/ thin films for DRAMs and integrated decoupling capacitors
Author(s): Basceri, C.; Wells, M.A.; Streiffer, S.K.; Kingon, A.I.; Bilodeau, S.; **Carl, R.**; Van Buskirk, P.C.; Summerfelt, S.R.; McIntyre, P.
Author Affiliation: Dept. of Mater. Sci. & Eng., North Carolina State Univ., Raleigh, NC, USA
Conference Title: ISAF '96. Proceedings of the Tenth IEEE International Symposium on Applications of Ferroelectrics (Cat. No.96CH35948) Part vol.1 p.51-4 vol.1

Editor(s): Kulwicki, B.M.; Amin, A.; Safari, A.
Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA 2 vol. 1034 pp.
ISBN: 0 7803 3355 1 Material Identity Number: XX97-01457
U.S. Copyright Clearance Center Code: 0 7803 3355 1/96/$5.00
Conference Title: ISAF '96. Proceedings of the Tenth IEEE International Symposium on Applications of Ferroelectrics
Conference Date: 18-21 Aug. 1996 Conference Location: East Brunswick, NJ, USA
Language: English
Abstract: We have investigated the important failure mechanism of resistance degradation for polycrystalline MOCVD (Ba,Sr)TiO/sub 3/ thin films appropriate for use in DRAMs, as a function of voltage (field), thickness and temperature. At constant field, the measured degradation lifetime decreases with increasing film thickness, resulting from a decrease in the activation energy with respect to temperature for thicker films. Similarly, there are clear indications that thicker films are more field sensitive. Predicted resistance degradation lifetimes obtained from both temperature and voltage extrapolations for DRAM operating conditions of 85 degrees C and 1.6 V exceed the current benchmark of 10 years for all the films studied.
Subfile: B

10/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5708143 INSPEC Abstract Number: B9711-1265D-008
Title: MOCVD BaSrTiO/sub 3/ for >or=1-Gbit DRAMs
Author(s): Bilodeau, S.M.; **Carl, R.**; Van Buskirk, P.; Ward, J.
Author Affiliation: Adv. Technol. Mater. Inc., Denbury, CT, USA
Journal: Solid State Technology vol.40, no.7 p.235, 237-8, 240, 242
Publisher: PennWell Publishing,
Publication Date: July 1997 Country of Publication: USA
CODEN: SSTEAP ISSN: 0038-111X
SICI: 0038-111X(199707)40:7L.235:MBGD;1-W
Material Identity Number: S046-97008
U.S. Copyright Clearance Center Code: 0038-111X/97/$1.00+.35
Language: English
Abstract: A CVD process for barium strontium titanate (BST) was developed to produce conformal thin films for 1 Gbit DRAMs. The process uses metal-organic precursors, liquid delivery, and point-of-use flash vaporization to obtain reproducible film stoichiometry. Good electrical results were achieved, including high storage density and low leakage currents at 1 Gbit DRAM operating voltages and temperatures. The process is both reproducible and robust.
Subfile: B

10/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5565281 INSPEC Abstract Number: B9706-1265D-004
Title: Thin **film** high k **dielectrics** for integrated passive devices

Author(s): Stauf, G.T.; **Carl, R.**; Bilodeau, S.; Van Buskirk, P.; Watts, K.
Author Affiliation: Adv. Technol. Mater. Inc., Danbury, CT, USA
Conference Title: Proceedings. 1996 International Symposium on Microelectronics (SPIE Vol.2920) p.349-54
Publisher: Microelectron. Soc, Reston, VA, USA
Publication Date: 1996 Country of Publication: USA xiii+610 pp.
ISBN: 0 930815 48 3 Material Identity Number: XX96-03083
Conference Title: 1996 International Symposium on Microelectronics
Conference Sponsor: Microelectron. Soc
Conference Date: 8-10 Oct. 1996 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: Over the last few years, there has been increasing interest in ferroelectric and related complex **oxide** thin **films** for a variety of applications. ATMI has developed a novel liquid delivery system for injection of low volatility chemical precursors into metalorganic chemical vapor deposition (MOCVD) reactors to produce these multicomponent **oxide** thin **films**, which include BaSrTiO/sub 3/ (BST), PbLaZrTiO/sub 3/ (PLZT) and other related materials. Of these materials, BaSrTiO/sub 3/ (BST) for integrated (DRAM) capacitors and memory elements has reached the highest state of maturity. We have integrated the liquid delivery system with a commercial reactor capable of producing highly uniform films on 6" Si wafers at high rates. Charge storage densities up to 6,000 nF/cm/sup 2/ have been attained using extremely thin **films** of BST. **Dielectric** constants range from 20 to over 500 depending on composition and processing, with Q factors as high as 500 at kHz frequencies and X7R or better temperature specification. We discuss the performance of BST at frequencies up to the GHz range, and its suitability for integrated passive devices at high frequencies, including switched capacitor filters and decoupling capacitors. There is also discussion of potential commercial markets and manufacturing feasibility for these materials.
Subfile: B

10/3,AB/5 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04937105
E.I. No: EIP98024060853
Title: MOCVD of advanced **dielectric** and ferroelectric **films** by liquid delivery
Author: Roeder, J.F.; Bilodeau, S.M.; **Carl, R.J. Jr.**; Gardiner, R.A.; van Buskirk, P.C.
Corporate Source: Advanced Technology Materials, Inc, Danbury, CT, USA
Conference Title: Proceedings of the 1997 9th International Symposium on Integrated Ferroelectrics. Part 2 (of 2)
Conference Location: Santa Fe, NM, USA Conference Date: 19970303-19970305
E.I. Conference No.: 47673
Source: Integrated Ferroelectrics v 18 n 1-4 pt 2 1997. p 109-118
Publication Year: 1997
CODEN: IFEREU ISSN: 1058-4587
Language: English
Abstract: An MOCVD technique has been developed for (Ba,Sr)TiO//3 (BST) films based on flash vaporization of metalorganic precursors with

exceptional composition control and no process drift for the equivalent of approx. 1300 wafers of 30 nm thickness. Charge storage density of greater than 60 fF/ mu m**2 has been routinely obtained for 30 nm films and values up to 100 fF/ mu m**2 have been observed for films with electrical leakage less than 10** minus **7 A/cm**2. The method has also been applied to other materials systems, including Pb(Zr,Ti)O//3 (PZT). High quality, single phase PZT films have been deposited and the effect of Zr/Ti ratio has been examined. Remanent polarization (P//r) and coercive field follow expected trends. P//r of approx. 20 mu C/cm**2 was observed with fully saturated hysteresis at 3V for films with 140-175 nm thickness. Coercive voltages less than 1V have also been obtained. This finding demonstrates promise of this deposition method for low voltage applications. (Author abstract) 10 Refs.

10/3,AB/6 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04368575
E.I. No: EIP96033112062
Title: Dielectric behavior of CVD (Ba,Sr)TiO//3 thin films on Pt/Si
Author: Streiffer, S.K.; Basceri, C.; Kingon, A.I.; Lipa, S.; Bilodeau, S.; **Carl, R.**; Van Buskirk, P.C.
Corporate Source: North Carolina State Univ, Raleigh, NC, USA
Conference Title: Proceedings of the 1995 MRS Fall Meeting
Conference Location: Boston, MA, USA Conference Date: 19951127-19951202
E.I. Conference No.: 44427
Source: Metal-Organic Chemical Vapor Deposition of Electronic Ceramics II Materials Research Society Symposium Proceedings v 415 1996. Materials Research Society, Pittsburgh, PA, USA. p 219-224
Publication Year: 1996
CODEN: MRSPDH ISSN: 0272-9172
Language: English
Abstract: We have investigated the dielectric behavior of polycrystalline (Ba,Sr)TiO//3 thin films deposited by liquid-source metalorganic chemical vapor deposition. The time-domain polarization current, the frequency dependence of the permittivity, and the dielectric loss for these CVD films are all described by a single set of parameters via the phenomenology of Curie - von Schweidler behavior. No change in the general form of the permittivity is found out to 1.5 GHz, suggesting that this description of the response is valid into the frequency range of interest for many applications. Low-frequency dispersion is found to be controllable, leading to films with very low dissipation factors and almost frequency-independent dielectric response. Finally, a non-zero intercept of the inverse of capacitance versus film thickness suggests the existence of a series interfacial capacitance, arising from either microstructural inhomogeneity or energy barriers to carrier transport at the film-electrode interfaces. (Author abstract) 12 Refs.

10/3,AB/7 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

02272334 INSIDE CONFERENCE ITEM ID: CN023782305
MOCVD of Polycrystalline and Epitaxial Complex Oxides by Liquid Delivery
Roeder, J. F.; Bilodeau, S. M.; **Carl, R. J.**; Baum, T. H.
CONFERENCE: Epitaxial oxide thin films III-Symposium

MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, 1997; VOL 474 P: 21-30
Pittsburgh, Pa., Materials Research Society, 1997
ISBN: 1558993789
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE EDITOR(S): Schlom, D. G.
CONFERENCE SPONSOR: Materials Research Society
CONFERENCE LOCATION: San Francisco, CA
CONFERENCE DATE: Mar 1997 (199703) (199703)

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L2              1 S E3
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L3              1 S E3
                E CHROMIUM/CN
L4              1 S E3
                E GOLD/CN
L5              1 S E3

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L4              1 S E3
                E GOLD/CN
L5              1 S E3
                E PLATINUM/CN
L6              1 S E3
                E PALLADIUM/CN
L7              1 S E3
                E GERMANIUM/CN
L8              1 S E3
                E SELENIUM/CN
L9              1 S E3

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L11       1274700 S (COPPER OR CU OR CHROMIUM OR CR ORGOLD OR AU)
L12        399837 S (PLATINUM OR PT OR PALLADIUM OR PD)
L13        258628 S (SELENIUM OR SE OR GERMANIUM OR GE)
L14           594 S ANTI(W)FUSE# OR ANTIFUSE# OR OTP OR ((ONE)(N)(TIME)(N)(PROGRA
L15        304029 S (DIELECTRIC? OR OXIDE OR INSULAT?)(3N)(FILM# OR LAYER? OR COA
L16        405538 S ((ANTI(N)REFLECT?)(2N)(COAT#### OR FILM# OR LAYER? OR MATERIA
                E COMPOUND SEMICONDUCTOR/CT
                E E4
                E E3+ALL/CT
L17           1120 S E2
                E CERAMICS/CT
L18          32533 S E3
                E E3+ALL/CT
L19       1032393 S (VIA OR VIAS OR TRENCH? OR HOLE? OR GROOVE# OR CHANNEL OR EDG
L20         42612 S (AMORPHOUS)(N)(SI OR SILICON OR C OR CARBON)

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L21             1 S E3

     FILE 'HCAPLUS' ENTERED AT 13:04:12 ON 08 JAN 2002
L22           158 S L14 AND L15
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L23          73 S L22 AND L19
L24          35 S L23 AND (L1-L7 OR L10 OR L10 OR L11 OR L12)
L25          31 S L23 AND (L8 OR L9 OR L13 OR L20 OR L16)

     FILE 'REGISTRY' ENTERED AT 13:10:23 ON 08 JAN 2002
L26         318 S (SI AND O AND N)/ELS AND 3/ELC.SUB
L27        1000 S (SILICON (N)NITRIDE(N) OXIDE) OR (SILICON (N)NITRIDE(N) OXIDE

     FILE 'HCAPLUS' ENTERED AT 13:29:12 ON 08 JAN 2002
L28           3 S L23 AND (L26 OR L27)
L29          49 S L24 OR L25 OR L28
L30          49 DUP REMOVE L29 (0 DUPLICATES REMOVED)
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L30 ANSWER 2 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:480738 HCAPLUS
DN 135:69609
TI Metal embedded passivation layer structure to fabricated fuses and **antifuses** for microelectronic interconnect formation, customization and repair
IN Bojarczuk, Nestor Alexander, Jr.; Guha, Supratik; Gupta, Arunava; Purushothaman, Sampath
PA International Business Machines Corporation, USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6255671	B1	20010703	US 1998-2840	19980105

AB A structure includes a metal nitride film MN, where M is selected from the group consisting of Ga, In, AlGa, AlIn, and AlGaIn. The structure has at least one elec. conductive metal region that is formed within and from the metal nitride film by a thermal process driven by absorption of light having a predetd. wavelength. Single films comprised of AlN are also within the scope of this invention, wherein an **Al** trace or interconnect is formed by laser radiation of wavelength 248 nm so as to contact circuitry that exists under the film. Multilayered stacks of films are also within the scope of the teachings of this invention. In this case each film layer may be sep. deposited and then illuminated to selectively form the desired elec. connection(s), which may also connect to conductive feature(s) in an underlying layer, or a plurality of metal nitride layers are stacked bottom to top in order of increasing electronic band gap energy value, and then the conductive features are written into selective ones of the layers by controlling the wavelength of the light to be absorbed in a desired layer. The teachings of this invention can be employed to fabricate fuses and **anti-fuses** enabling selective circuit customization, test and repair. Also disclosed is a technique for forming elec. resistors in a metal nitride layer by adjusting the elec. resistance of the metalization formed from the metal nitride film layer.

L30 ANSWER 6 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:329953 HCAPLUS
DN 130:331420
TI Programmable **anti-fuses** fabricated using laser writing
IN Thomas, Michael E.
PA National Semiconductor Corporation, USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5904507	A	19990518	US 1998-28190	19980223

AB Disclosed is a method of fabricating a programmable **antifuse** structure wherein programming of the **antifuse** structure results in conducting paths which are confined within a finite predictable area. The method includes depositing an **insulating layer** over a field **oxide**. Addnl., the method includes creating a **via** through a **via** area of the **insulating layer** to expose a programmable surface area of the field. The method also includes depositing an interlayer over the exposed programmable surface of the field, over sidewalls of the **via**, and over an extended surface region of the **insulating layer**, the extended surface region including the **via** area. The method includes depositing a 1st conducting layer over the interlayer. The method also includes etching in the extended surface region to the **insulating layer**; the etching is for confining formation of conductive paths to within the **via** area upon programming of the programmable **antifuse** structure. The method further includes depositing a 2nd conducting layer over the **via** area.

L30 ANSWER 9 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:534954 HCAPLUS
DN 129:169168
TI **Antifuse** structure on semiconductor substrate and fabrication thereof
IN Sanchez, Ivan; Han, Yu-Pin; Delgado, Miguel A.; Loh, Ying-tsong
PA Vlsi Technology, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5789795	A	19980804	US 1995-579824	19951228

AB An integrated circuit having a semiconductor substrate and an **antifuse** structure formed on the semiconductor substrate. The **antifuse** structure includes a metal-one layer and an **antifuse** layer disposed above the metal-one layer. The **antifuse** layer has a first resistance value when the **antifuse** structure is unprogrammed and a second resistance value lower than the first resistance value when the **antifuse** structure is programmed. There is further provided an etch stop layer disposed above the **antifuse** layer, and an inter-metal **oxide layer** disposed above the etch stop layer with the inter-metal **oxide layer** has a **via** formed therein. Addnl., there is further provided a metal-two layer disposed above the inter-metal **oxide layer**. In this structure, a portion of the metal-two layer is in elec. contact with the **anti -fuse** layer through the **via** in the inter-metal **oxide layer**.

L30 ANSWER 10 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:157394 HCAPLUS
DN 128:211815
TI Integrated circuit having **amorphous silicon antifuse** structures and its manufacture
IN Manley, Martin Harold
PA VLSI Technology, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5723358	A	19980303	US 1996-639557	19960429
	US 5962911	A	19991005	US 1997-941512	19970930
PRAI	US 1996-639557		19960429		

AB **Antifuse** structures are formed over topog. lower Si substrate regions such that subsequent **via hole** etching processes do not overetch the underlying **antifuse** structures. Dummy metalization and polysilicon features are formed in close proximity to **antifuse** structures such that subsequently deposited **dielec. materials** are induced to form thicker **dielec. layers** over the **antifuse** structures. Advantageously, subsequent **via hole** etching does not substantially remove **antifuse** structure materials which may cause detrimental ionic contamination or destruction of the **antifuse**. In this manner, std. **via hole** etching techniques may be implemented for all interlayer **via holes** without the concern of overetching sensitive underlying devices.

L30 ANSWER 12 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:607555 HCAPLUS
DN 125:236087
TI **Antifuse** with a double-**via** spacer-defined contact and its manufacture
IN Iranmanesh, Ali
PA Crosspoint Solutions, Inc., USA
SO PCT Int. Appl., 25 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9625766	A1	19960822	WO 1996-US2024	19960209
	W: JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 5663591	A	19970902	US 1995-388673	19950214
PRAI	US 1995-388673		19950214		

AB The present invention provides for a method of forming an **antifuse** in an integrated circuit having a 1st **insulating layer** on a semiconductor substrate. The method comprises forming a 1st metal interconnection **layer** on the 1st **insulating layer**; forming a relatively thin, 2nd **insulating layer** over the 1st metal interconnection layer with a **via** where the **antifuse** is to be located to expose the 1st metal interconnection layer; forming 1st spacer regions on the sidewalls of the 2nd **insulating layer**; forming a programming **layer** on the 2nd **insulating layer** and in the **via** to contact the 1st metal interconnection line; forming 2nd spacer regions on the sidewalls of the programming layer in the **via**; forming a barrier metal layer on the programming layer; forming a relatively thick, 3rd **insulating layer** on the barrier metal layer with a 2nd aperture to expose a portion of the barrier metal layer; and forming a 2nd metal interconnection **layer** on the 3rd **insulating layer** and in the 2nd aperture to contact the portion of the barrier metal layer.

L30 ANSWER 14 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:172265 HCAPLUS
DN 124:247990
TI **Anti-fuse** structure for reducing contamination of the **anti-fuse** material
IN Pramanik, Dipankar; Nariani, Subhash R.
PA Vlsi Technology, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5493146	A	19960220	US 1994-275187	19940714
	US 5573970	A	19961112	US 1995-477311	19950606
	US 36893	E	20001003	US 1997-795098	19970206
PRAI	US 1994-275187	A3	19940714		

AB The **anti-fuse** structure includes a conductive base layer. A layer of **anti-fuse** material overlies the conductive base layer. On top of the **anti-fuse layer** is an **insulating layer**, in which a **via hole** is formed to the **anti-fuse** layer. The lateral dimension of the **via hole** is .ltorsim.0.8 .mu.m. Provided in the **via hole** is a conductive non-**Al** plug including a conductive barrier material such as TiN or TiW to contact the **anti-fuse material** and overlie the **insulating layer**. **W** is effectively used as the non-**Al** plug. An elec. conductive layer is formed over the plug and is sepd. from the **anti-fuse** layer by .gtoreq.1/2 the depth of the **via hole**. The structure is then programmable by application of a programming voltage and readable by application of a sensing voltage, which is lower than the programming voltage.

L30 ANSWER 16 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:140559 HCAPLUS
DN 126:151679
TI **Antifuse** device with good programming characteristics and its manufacture
IN Ishida, Tetsuo
PA Matsushita Electronics Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08330430	A2	19961213	JP 1995-131547	19950530

AB The device, including a 1st wiring layer of **Al** (or Ti) or its compd. **coated** with an interlayer **insulating film** and with a 2nd wiring layer, contains a metal-filled **via hole** in the **insulating film** reaching to the 1st wiring layer, where an **antifuse** layer of AlF3 (or Ti fluoride) is formed at the **via-hole** bottom. The manuf., including formation of the **antifuse** layer by reaction of the 1st wiring layer, exposed at bottom of the **via**

-**hole**, with a metal fluoride gas, is also claimed. The as-manufd. device with an **antifuse** layer of uniform thickness shows high reliability.

L30 ANSWER 17 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:129847 HCAPLUS
DN 126:151549
TI Semiconductor devices with decreased power consumption
IN Akanuma, Hideyuki
PA Seiko Epson Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08316428	A2	19961129	JP 1995-122815	19950522

AB The devices, having **anti-fuse** elements, consist of a semiconductor layer or a 1st metal wiring **layer**, a 1st **insulation layer**, a conjunction **hole** opened at the **insulation layer**, a 2nd **insulation layer** partially covered on the bottom of the junction **hole**, an **amorphous Si** layer over the bottom of the junction **hole** (at least the part not covered with the **insulation layer**), and a 2nd metal wiring layer.

L30 ANSWER 18 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:645686 HCAPLUS
DN 125:290809
TI Semiconductor integrated circuit device having **anti-fuse** element and its manufacture
IN Jinriki, Hiroshi; Tamura, Yoshimitsu; Oota, Tomohiro
PA Kawasaki Steel Co, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 08222637	A2	19960830	JP 1995-22448	19950210

AB The **anti-fuse** element consists of an **insulating film** for an **anti-fuse** between a lower electrode which is manufd. on a metal silicide film on p-type semiconductor region and an upper electrode. The p-type semiconductor region is manufd. by the method in fabricating p-**channel** MISFET source/drain or p-type gate. The manuf. of the device involving the silicide formation is also claimed. The device is useful for field programmable gate array, PROM, etc.

L30 ANSWER 19 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:551149 HCAPLUS
DN 125:210272
TI **Antifuse** semiconductor integrated circuits
IN Jinriki, Hiroshi; Tamura, Yoshimitsu; Kimura, Yoshitaka; Tsutsui, Che; Oota, Tomohiro; Komya, Takayuki
PA Kawasaki Steel Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 38 pp.

CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08153799	A2	19960611	JP 1995-210670	19950818
	JP 3104843	B2	20001030		
	US 5565702	A	19961015	US 1994-353296	19941205
	US 5641985	A	19970624	US 1994-353294	19941205
	US 5679974	A	19971021	US 1994-353287	19941205
PRAI	JP 1994-195690	A1	19940819		
	JP 1994-235057	A1	19940929		
	JP 1994-235058	A1	19940929		
	JP 1994-235059	A1	19940929		
	US 1994-353287	A	19941205		
	US 1994-353294	A	19941205		
	US 1994-353296	A	19941205		

AB The circuit has its lower layer electrodes made of an amorphous conductive material. The upper layer electrode may be made of an amorphous conductive material. The conductive material may be (1) a compd. from .apprx.>2 of Co, Ni, **Cu**, Ti, Zr, Nb, Mo, Hf, Ta, and **W** (group 1), (2) a compd. from .apprx.>1 of Group 1 with .apprx.>1 of Si, B, N, C, **Ge**, As, P, and Sb (Group 2), or **Al**, or Y and/or La, and **Al**, (3) Y-La or a compd. from Y and/or La with **Al**, or (4) a compd. from **Au**, **Pt**, **Pd**, and/or Ag with .apprx.>1 of Group 2, .apprx.>1 of Group 1, or Y and/or La. The lower layer electrode may be a metal silicide with compn. ratio of the metal higher than the stoichiometric ratio. The lower and the upper layer electrode may be formed from a material contg. refractory metal(s) and a low m.p. metal lower in resistivity than the refractory metal(s), resp. The circuit may have (1) the lower wiring layer consisting of an **Al** alloy film and the uppermost layer of TiN, the lower layer electrode from the **Al** alloy film with removal of the TiN film in the depth direction at the bottom of the contact **hole**, **antifuse insulating films** from a SiO2, a Si3N4, or a Ta2O5 film, and the upper layer electrode with the lowermost layer from an **Al** alloy which forms a contact to **antifuse insulating film** of the upper wiring, or (2) the lower layer electrode forming a contact of the lower wiring from an **Al** or an **Al** alloy monolayer to the **antifuse insulating film**, the upper **layer** electrode from **Al** or an **Al** alloy, and the lower wiring located immediately above an **insulating film** on the substrate and elec. connected to the substrate in a contact **hole** through a barrier metal composite film.

L30 ANSWER 21 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:248261 HCAPLUS
DN 124:304400
TI Semiconductor integrated circuit having **antifuse amorphous silicon** and its manufacture
IN Yoshiura, Aimei; Ootaka, Akira
PA Hitachi Ltd, Japan; Hitachi Micro System Kk
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08031941	A2	19960202	JP 1994-159847	19940712

AB The circuit has a 1st 3-layered wiring layer, the surface of which is selectively oxidized and coated with an **antifuse amorphous Si** film, and a 2nd 3-layered wiring layer connected to the **amorphous Si** film. The 1st and 2nd wiring layers may consist of a 1st metal layer and a 3rd metal layer comprising a Ti compd., Ti, or TiSi and a 2nd metal layer comprising **Al** or **Al** alloy. The metal **oxide film** and the **amorphous Si** film may be formed on the field **oxide film**. The manuf. involves forming a 1st wiring **layer**, forming an **insulator** with a **via hole** on the wiring layer, selectively oxidizing the bottom surface (a 3rd metal layer) of the **via hole**, forming an **antifuse amorphous Si film** on the metal **oxide film**, and forming a 2nd wiring layer over the **via hole**. The **amorphous Si** film has a small leak current and a large fuse contact voltage.

L30 ANSWER 23 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:46867 HCAPLUS
DN 124:74116
TI A low-capacitance, plugged **antifuse** and its manufacture
IN Iranmanesh, Ali
PA Crosspoint Solutions, Inc., USA
SO PCT Int. Appl., 19 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9532522	A1	19951130	WO 1995-US6625	19950524
	W: JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 5521440	A	19960528	US 1994-248789	19940525
PRAI	US 1994-248789		19940525		

AB An **antifuse** structure for an integrated circuit has a 1st metal interconnection line and a 1st **insulating layer** formed over the 1st metal interconnection line. The 1st **insulating layer** has a **via** exposing the top surface of the 1st metal interconnection line. In the 1st aperture, a metal plug is made to contact the 1st metal interconnection layer and has a top surface formed substantially coplanar with the top surface of the 1st **insulating layer**. A metal pad contacts and covers the top surface of the metal plug. The metal pad should be formed by a viscous barrier metal, such as TiW, to smooth the surface of the metal plug. A 2nd **insulating layer**, relatively thin with respect to the 1st **insulating layer**, covers the metal pad. A programming layer is deposited over the 2nd **insulating layer** and into the aperture to contact the top surface of the metal pad. A 2nd metal interconnection line is formed on the programming layer.

L30 ANSWER 25 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:705714 HCAPLUS
DN 123:129908
TI Making a multilevel **antifuse** structure
IN Chang, Kuang Yeh
PA VLSI Technology, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5427979	A	19950627	US 1993-138298	19931018
	IL 111308	A1	19970713	IL 1994-111308	19941014
	US 5565703	A	19961015	US 1995-415182	19950403
PRAI	US 1993-138298		19931018		

AB A multilevel **antifuse** structure comprises a substrate, a 1st **antifuse** structure formed above the substrate, and a 2nd **antifuse** structure formed above the 1st **antifuse** structure. The 1st **antifuse** structure preferably includes a 1st conductive layer, a 1st **antifuse** layer disposed over the 1st conductive **layer**, a 1st **dielec. layer** disposed over the 1st **antifuse** layer and provided with a 1st **via hole**, and a 1st conductive **via** formed within the 1st **via hole**. The 2nd **antifuse** structure preferably includes a 2nd conductive layer, a 2nd **antifuse** layer disposed over the 2nd conductive **layer**, a 2nd **dielec. layer** disposed over the 2nd **antifuse** layer and provided with a 2nd **via hole** , and a 2nd conductive **via** formed within the 2nd **via hole**. Preferably, the 1st **antifuse** layer and the 2nd **antifuse** layer are patterned into a plurality of **antifuse** regions which are either vertically aligned or vertically staggered with respect to each other. A method for making a multilevel **antifuse** structure in accordance with the present invention includes the steps of forming a 1st **antifuse** structure over a substrate, and forming a 2nd **antifuse** structure over the 1st **antifuse** structure. In 1 embodiment, the 1st **antifuse** structure and the 2nd **antifuse** structure are vertically aligned, and are interconnected in parallel. The parallel interconnection is preferably accomplished by **W vias** formed by either a blanket **W** deposition and subsequent etch-back, or by a selective **W** deposition.

L30 ANSWER 26 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:546820 HCAPLUS
DN 122:279970
TI Wet/dry **antifuse via** etch
IN Delgado, Miguel A.; Hall, Stacy W.
PA VLSI Technology, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI US 5391513 A 19950221 US 1993-171590 19931222
AB In forming **vias** in an **antifuse** semiconductor device through an **oxide layer** to an underlying metallic layer, a wet etch is performed on the **oxide layer** at selected regions where **vias** are to be formed. The wet etch is controlled such that a 1st recessed area is formed in the **oxide layer** at the selected regions. The 1st recessed area formed by the wet etch extends only partially through the **oxide layer** toward the underlying metallic layer. Addnl., the 1st recessed area is formed having a smoothly shaped contour. Next, a dry etch is performed on the **oxide layer** at the selected regions where the **vias** are to be formed. The dry etch is performed within the 1st recessed area. The 2nd recessed area has a smaller cross sectional area than the 1st recessed area such that the 2nd recessed area is peripherally bordered by the 1st recessed area. The 2nd recessed area extends from the bottom of the 1st recessed area completely through the remaining **oxide layer** to the underlying metallic layer. In so doing, when **amorphous Si** is deposited into the **vias**, cusping of the **amorphous Si** within the **vias** is substantially reduced. As a result, the step of depositing a spacer oxide to fill in notches created by cusping of the **amorphous Si** layer is eliminated. Consequently, when the **amorphous Si** is removed or etched from selected strap **vias**, because no spacer oxide has been deposited, no deleterious residue or "dog ears" of **amorphous Si** remain within the strap **vias**.

L30 ANSWER 31 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:448180 HCAPLUS
DN 121:48180
TI Fabricating an above-**via** metal-to-metal **antifuse**
IN Hawley, Frank W.; Yeouchung, Yen
PA Acetal Corp., USA
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5308795	A	19940503	US 1992-971734	19921104

AB A method for fabricating a metal-to-metal **antifuse** comprises the steps of forming and defining a 1st metal interconnect **layer**; forming an interlayer **dielec. layer**; forming an **antifuse via** in the **dielec. layer** to expose the 1st metal interconnect layer; depositing a **via** metal layer into a portion of the vol. defining the **antifuse via**; forming a planarizing **layer** of an **insulating material** in the **antifuse via** sufficient to fill the remaining portion of the vol. defining the **antifuse via**; etching the planarizing layer to expose the upper surface of the **via** metal layer and the upper surface of the **dielec. layer** to form a substantially planar surface comprising the upper surface of the **dielec. layer**, the planarizing **layer**, and the upper surface of the **via** metal layer; forming an **antifuse** material layer over the substantially planar surface; forming a metal capping layer over the **antifuse** material layer; and defining the **antifuse** material layer and the metal capping layer.

L30 ANSWER 32 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:448274 HCAPLUS
DN 121:48274
TI Forming a metal-to-metal **antifuse** structure on a semiconductor device
IN Tigelaar, Howard L.; Misium, George
PA Texas Instruments Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5300456	A	19940405	US 1993-79194	19930617
	US 5451810	A	19950919	US 1993-166429	19931214
	JP 07142585	A2	19950602	JP 1994-135931	19940617
PRAI	US 1993-79194		19930617		

AB An **antifuse** stack is formed comprising a 1st metal **layer**, an **antifuse dielec. layer**, and an etch stop layer. The etch stop layer may, e.g., comprise an **oxide layer** and an **amorphous Si** layer. An **antifuse via** is etched through an interlevel **dielec. layer** to the **antifuse** stack. Next, a portion of the etch stop layer at the bottom of the **via** is removed. Finally, a 2nd layer of metal is deposited to fill the **antifuse via** and etched to form the desired interconnections.

L30 ANSWER 34 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:667103 HCAPLUS
DN 123:72169
TI Semiconductor devices with **anti-fuses**
IN Jinriki, Hiroshi; Kaizuka, Kenji; Oota, Tomohiro
PA Kawasaki Steel Co, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06310604	A2	19941104	JP 1993-92961	19930420

AB The **anti-fuses** consist of lower and upper interconnections, interlayer **insulator films** with contact **holes**, **insulator films** formed in the contact **holes** and insulating the 2 interconnections. The **insulator films** are made of Ge10Te50As30, which become elec. conductive upon application of writing voltage, and elec. connect the 2 interconnections.

L30 ANSWER 36 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:557155 HCAPLUS
DN 122:304259
TI Formation of **amorphous silicon antifuses** in semiconductor devices
IN Mizutani, Hiroshi; Sekine, Hiroaki
PA Fujitsu Ltd, Japan; Fujitsu Vlsi Ltd
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06268071	A2	19940922	JP 1993-52778	19930315

AB The process involves forming an under-layer circuit on a substrate, depositing an **insulator film** over the circuit, opening a contact **hole** to the **insulator film** to expose the circuit, depositing an **amorphous Si** thin-film formed on the bottom of the contact **hole**, forming a diffusion resistance film over the Si thin-film, and forming an upper-layer circuit to fill the contact **hole** to provide an **antifuse** with the **amorphous Si** thin-layer. The side-**edges** of the thin-film is oxidized before the deposition of the diffusion resistance film.

L30 ANSWER 37 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:529935 HCAPLUS
DN 119:129935
TI **Anti-fuse** structures and their manufacture
IN Boardman, William J.; Chan, David P. Kwan; Chang, Kuang Yeh; Gabriel, Calvin T.; Jain, Vivek; Nariani, Subhash R.
PA VLSI Technology, Inc., USA
SO PCT Int. Appl., 21 pp.
CODEN: PIXXD2

DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9305514	A1	19930318	WO 1992-US7453	19920903
	W: JP, KR				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, SE				
	US 5328865	A	19940712	US 1993-11084	19930129
PRAI	US 1991-755259		19910904		

AB A method for making an **anti-fuse** structure is characterized by the steps of forming a conductive base layer; forming an **anti-fuse** layer over the base layer; patterning the **anti-fuse** layer to form an **anti-fuse** island; forming an **insulating layer** over the **anti-fuse** island; forming a **via hole** through the **insulating layer** to the **anti-fuse** island; forming a conductive connection **layer** over the **insulating layer** and within the **via hole**; and patterning the conductive connection layer to form a conductive contact to the **anti-fuse** island. Preferably, the **anti-fuse** island comprises **amorphous Si** which can optionally be covered with a thin layer of a Ti-**W** alloy.

L30 ANSWER 38 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:593742 HCAPLUS
DN 119:193742
TI Manufacture of semiconductor devices
IN Tsuzuki, Norihisa
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05190677	A2	19930730	JP 1992-2832	19920110

AB In multilayered wirings having contact **holes** comprising **amorphous Si**: **amorphous Si** is deposited, covering some of the contact **holes** formed in interlayer **insulators**; 1st barrier metal **layer** is formed; the Si and the barrier metal layers are patterned so as to cover the contact **holes** entirely; pretreated under dry conditions; 2nd barrier metals are formed completely over the substrate; and then the upper wirings are deposited. The method is useful for fabrication of field programmable gate arrays.

L30 ANSWER 39 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:43801 HCAPLUS
DN 120:43801
TI Semiconductor devices having an **anti-fuse**
IN Saito, Tomyasu
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05121557	A2	19930518	JP 1991-282411	19911029

AB Title device comprises (1) a lower circuit layer formed on a semiconductor substrate, (2) a contact-**holed insulator film** formed over the lower circuit layer, and (3) an upper circuit **layer** formed on the **insulator film** and connected to the lower circuit layer through the contact **hole**; wherein a portion of the upper or lower circuit layer is elec.-disconnected and filled with an **amorphous Si** in the disconnected portion. Arrangement makes simplified formation of the **anti-fuse** with a stable and quality-controlled properties.

L30 ANSWER 42 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:43802 HCAPLUS
DN 120:43802
TI Semiconductor devices having an **anti-fuse** and fabrication thereof
IN Yokoyama, Junichi
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05121554	A2	19930518	JP 1991-281717	19911028

AB Title fabrication involves (1) forming a highly-doped region on a Si substrate, (2) forming an **insulator film** on the substrate, (3) opening a contact **hole** to the **insulator film** to expose the doped region, (4) forming a refractory metal layer over the contact **hole**, (5) heating to form a silicide by a reaction between the doped region and the refractory metal layer to give a refractory metal silicide layer on the doped region, (6) forming an **amorphous Si** layer on the silicide layer, and (7) subsequently forming a metal contact on the amorphous layer. The fabrication provides an **anti-fuse** formation without its deterioration which may otherwise be caused by etching.

L30 ANSWER 46 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:593531 HCAPLUS
DN 119:193531
TI Manufacture of integrated circuits containing **antifuses**
IN Shimizu, Katsunori
PA Fujitsu Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05029466	A2	19930205	JP 1991-180008	19910720

AB The process includes (a) thermally oxidizing a Si substrate to form an **oxide film** on it; (b) forming a borophosphosilicate glass **film** on the **oxide film**; (c) etching the glass **film** and the **oxide film** to create through **holes**; (d) selectively growing **W** in the through **holes**; (e) forming a Ti film on the whole surface; (f) heating the substrate to form a Ti-**W** alloy film on the through **holes**; (g) removing the Ti film on the substrate, leaving the Ti-**W** alloy film; and (h) forming an **amorphous Si** film on the substrate, and selectively etching it to form a pattern on the Ti-**W** alloy film, creating a circuit which becomes elec. connected by running elec. current.

L30 ANSWER 47 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:639513 HCAPLUS
DN 119:239513

TI Semiconductor device with **antifuse** and production method
IN Saiki, Takashi; Mochizuki, Akitoshi; Tsuzuki, Norihisa
PA Fujitsu Ltd., Japan
SO Eur. Pat. Appl., 23 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 539197	A1	19930428	EP 1992-309651	19921022
	R: DE, FR, GB				
	JP 05198681	A2	19930806	JP 1992-281356	19921020
PRAI	JP 1991-275822		19911023		
	JP 1991-275823		19911023		
	JP 1991-278206		19911025		

AB A semiconductor device (e.g., FPGA, PROM), with an **anti-fuse**, comprises a semiconductor substrate; an **insulating layer** formed on the semiconductor substrate; a lower wiring **layer** formed above the **insulating layer**; an amorphous semiconductor layer formed above the lower wiring **layer** ; an interlaminar **insulating layer** which is formed on the **insulating layer** and the amorphous semiconductor layer and has contact **holes** reaching the amorphous semiconductor layer; and an upper wiring layer which is formed on the interlaminar **insulating layer** and is connected to the amorphous semiconductor layer through the contact **hole**. When the lower wiring layer and the upper wiring layer are **Al** preferably, a lower barrier layer and an upper barrier layer are formed between the amorphous semiconductor layer and the lower and upper wiring layers, resp.

L30 ANSWER 48 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1993:245858 HCAPLUS
DN 118:245858
TI Manufacture of **antifuse** semicondcutor device and gate-array device
PA Maizan Technology Inc., USA; Naitsu Technology Inc.
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04315468	A2	19921106	JP 1992-8944	19920122
PRAI	US 1991-644231		19910122		

AB The title manuf. using conventional method until a contact **hole** is formed comprises the steps of depositing and patterning a 1st layer from Ti (or heat-resistant metal) or a metal silicide, depositing an **insulating film**, forming a **via**-contact opening in the **insulating film**, etching the metal film through the opening, depositing an **amorphous Si**-based **insulating antifuse layer** with 30-400 nm thickness at .ltoreq.500.degree., etching the **antifuse** layer through a mask, and depositing a 2nd heat-resistant metal or metal silicide layer. This **antifuse** semiconductor device is used for a programmable ROM (PROM) and an application specific integrated circuit (ASIC). The gate-array device was also claimed.

L30 ANSWER 49 OF 49 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:507492 HCAPLUS
DN 113:107492
TI Semiconductor **antifuse** structure and method
IN Gordon, Kathryn E.; Jenq, Ching S.
PA Advanced Micro Devices, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4914055	A	19900403	US 1989-398141	19890824
	JP 03179763	A2	19910805	JP 1990-213576	19900809
PRAI	US 1989-398141		19890824		

AB A method is described for forming an array of **antifuse** structures on a semiconductor substrate which previously has had complementary MOS devices fabricated on it up to 1st metalization. A fuse structure is formed as a sandwich by successively depositing a bottom layer of TiW, a layer of **amorphous Si**, and a top layer of TiW. The **amorphous Si** is formed in an **antifuse via** formed in a **dielec. layer** covering the bottom layer of TiW. First metalization is deposited and patterned over the top layer of TiW. An intermetal **dielec. layer** is formed over the fuse array and 2nd metal conductors are formed thereon. Alternatively, an oxide sidewall spacer may be formed around the periphery of the **antifuse** structure. Connection resistance to the bottom layer of TiW is lowered by using a no. of **vias** between the 2nd-metal conductors and the bottom layer of TiW in a row of an array of **antifuse** devices.

SYSTEM:OS - DIALOG OneSearch
File 350:Derwent WPIX 1963-2001/UD,UM &UP=200201
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*File 350: Price changes as of 1/1/02. Please see HELP RATES 350.
More updates in 2002. Please see HELP NEWS 350.
File 347:JAPIO OCT 1976-2001/Aug(UPDATED 011203)
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*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run. See HELP NEWS 347 for details.

Set	Items	Description
S1	7	AU="CARL R" OR AU="CARL R J"

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1/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013492138
WPI Acc No: 2000-664081/200064
XRAM Acc No: C00-201103
XRPX Acc No: N00-492086
Formation of parylene film for microelectronic device fabrication, involves flash vaporizing and cracking precursor, and contacting precursor vapor with substrate for condensing monomer and/or reactive species
Patent Assignee: ADVANCED TECHNOLOGY MATERIALS (ADTE-N)
Inventor: BAUM T H; **CARL R J**; STURM E A; XU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6123993	A	20000926	US 98157966	A	19980921	200064	B

Priority Applications (No Type Date): US 98157966 A 19980921
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6123993	A		15	C23C-016/448	

Abstract (Basic): US 6123993 A
Abstract (Basic):

NOVELTY - A liquid phase precursor comprising a parylene source reagent liquid or solvent solution of reagent, is subjected to flash vaporization in a flash vaporizer cracking unit. The flash vaporized precursor is cracked in the vaporizing unit. The precursor vapor is contacted with a substrate (52) under conditions which produce condensation of the monomer and/or reactive species, to form a parylene film (50).

DETAILED DESCRIPTION - A liquid phase precursor comprising a parylene source reagent liquid or solvent solution of reagent, is subjected to flash vaporization in a flash vaporizer cracking unit. The flash vaporized precursor is pyrolytically cracked in the vaporizing unit, to form precursor vapor containing parylene source monomer and/or reactive radical species. The precursor is contacted with a substrate under conditions which produce condensation of the monomer and/or reactive species, to form a parylene film on the substrate.

USE - For fabrication of microelectronic devices such as very large scale integration devices.

ADVANTAGE - A thermally conductive high surface area medium is used which serves both as a vaporization matrix and flow restriction matrix, to induce turbulence in precursor vapor flow and increase in the residence time. Parylene thin film is obtained with high efficiency.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic representation of the cross-section of the cracking zone of the vaporizing unit.

Parylene film (15)

Substrate (52)

pp; 15 DwgNo 2/8

1/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012264579
WPI Acc No: 1999-070685/199906
XRAM Acc No: C99-021099
XRPX Acc No: N99-051608

Delivery of liquid reagent in vaporised form to a reactor - with in-situ cleaning using heaters to remove deposited decomposition by-product material

Patent Assignee: ADVANCED TECHNOLOGY MATERIALS (ADTE-N)
Inventor: BILODEAU S M; **CARL R J**; VAN BUSKIRK P C
Number of Countries: 080 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9858096	A1	19981223	WO 98US12539	A	19980617	199906	B
US 5882416	A	19990316	US 97878616	A	19970619	199918	
AU 9880734	A	19990104	AU 9880734	A	19980617	199921	
KR 2001013933	A	20010226	KR 99711955	A	19991217	200154	

Priority Applications (No Type Date): US 97878616 A 19970619
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9858096	A1	E	38	C23C-016/00	
US 5882416	A			C23C-016/00	
AU 9880734	A			C23C-016/00	Based on patent WO 9858096
KR 2001013933	A			C23C-016/00	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

Abstract (Basic): WO 9858096 A

A liquid delivery system for delivery of an initially liquid reagent in vaporised form to a chemical vapor deposition reactor comprises an elongated vaporisation fluid flow passage (130), a vaporisation element (120) contained within the fluid flow passage transverse to the longitudinal axis, a source reagent liquid feed passage (122) having a terminus arranged to discharge liquid in a direction perpendicular to a facing surface of the vaporisation element (120), a heater for heating the vaporisation element to a temperature for vaporisation of the liquid reagent and a manifold (137) for flowing vapor to the chemical vapor deposition reactor, in which the manifold including a diverting means (138) to prevent non-volatile residue from

flowing to the reactor. Several heaters may be employed to heat various components.

USE - Delivering an initially liquid reagent in vaporised form to a chemical vapor deposition reactor to prevent the undesired accumulation of non-volatile residues in the vaporisation zone.

ADVANTAGE - The cleaning method is effective in removing the deposited decomposition by-product material in the vaporisation zone and also in any additional flow circuit portions such as conduit, valves and interior surfaces.

Dwg.1/6

1/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011972220
WPI Acc No: 1998-389130/199834
XRAM Acc No: C98-117805
XRPX Acc No: N98-303487

Electro-optical coupler with circuitry and converters, separated from optical fibres by filled coupling gap - has wavelength-specific silicone material gap filler introduced easily because of low initial viscosity, and is surrounded by similar, but opaque material which keeps moisture out

Patent Assignee: SIEMENS AG (SIEI)
Inventor: **CARL R**; LEHNER B; PLICKERT V
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 19714170	C1	19980730	DE 1014170	A	19970321	199834	B
US 5940550	A	19990817	US 9847165	A	19980323	199939	

Priority Applications (No Type Date): DE 1014170 A 19970321
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 19714170	C1		4	G02B-006/42	
US 5940550	A			G02B-006/26	

Abstract (Basic): DE 19714170 C

The novel electro-optical coupler for optical fibres has a converter (1) with optically-active regions coupled individually to optical fibres, forming coupling gaps. A light-sensitive integrated electronic circuit (14) is located near the converter. This is electrically wire-bonded to the converter. A first material (20) specific to the light converted, fills each coupling gap. A second material (26) surrounds the circuit. This is basically of the same composition as the first material, but its optical characteristics are modified to make it e.g. opaque or reflective to the light affecting the circuit. First and second materials share a common boundary surface (24), through which the connecting wires (8 g) pass.

USE - An electronic opto-coupler for data.

ADVANTAGE - The coupling region of each fibre is critical and needs to be protected from external influences, e.g. moisture and temperature change. This coupler achieves reliable, multi-channel protection for the gaps. Operation at high frequencies is achieved by virtue of close coupling in the smallest space. Use of basically similar materials (chemically and structurally) to form the interface, assures mechanical homogeneity avoiding e.g. differential thermal stresses on the

components and especially on the bonding wires. Processing is also simplified. A range of light screening or absorbing fillers is suggested. Use of silicone material confers extreme temperature resistance; its low viscosity assures excellent gap filling.
Dwg.1/3

1/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010857743
WPI Acc No: 1996-354696/199635
XRPX Acc No: N96-299058
24 hour analogue watch - has dual display
Patent Assignee: CARL R (CARL-I)
Inventor: **CARL R**
Number of Countries: 019 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9622566	A1	19960725	WO 94EP3842	A	19950118	199635	B

Priority Applications (No Type Date): WO 94EP3842 A 19950118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9622566	A1	G	8	G04G-009/00	

Designated States (National): CN JP US
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

Abstract (Basic): WO 9622566 A
This international patent application requests protection for the right to produce, distribute/sell 24 hour analogue/digital watches in the form of wrist and pocket watches, radio, car, grandfather and wall clocks.
ADVANTAGE - Immediate recognition of actual time whether day or night.
Dwg.1/1

1/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003395524
WPI Acc No: 1982-Q1784E/198246
Rail truck bolster unit - has flange and wear ring with cut-away sections filled with hardened alloy by welding
Patent Assignee: WEAR C W (WEAR-I)
Inventor: **CARL R J**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4356774	A	19821102				198246	B

Priority Applications (No Type Date): US 80122574 A 19800219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4356774	A		3		

Abstract (Basic): US 4356774 A

The truck bolster has the bolster ring (12) mounted by welding to form an upstanding flange.

The inner liner of the flange which is adapted to contact a centre post is separately referred to as wear resistant material (22). Ring (12) is of a steel material and has inner and outer diameters (14 and 16) respectively. The ring is also cut away at (18 and 20) and is positioned on a bolster (10) and the cut-away areas (18 and 20) are filled with a suitable welding material (23) to weld the ring to the bolster.

1,2,3/3

1/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003339114
WPI Acc No: 1982-J7131E/198229
Coded data transmission system - has recorder which registers connection of receiver decoder via signal channel to encoder control
Patent Assignee: WERN C R (WERN-I)
Inventor: **CARL R**; GEORGE H; LARS A
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SE 8007165	A	19820517				198229	B
SE 451104	B	19870831				198737	

Priority Applications (No Type Date): SE 807165 A 19801013
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SE 8007165	A		14		

Abstract (Basic): SE 8007165 A

The data transmission system comprises a transmitter with an attached encoder. It has a control input, controls for the encoder, and a receiver which receives the encoded data from the transmitter via a data channel. The receiver has a decoder unit. The decoder has a control input connected to the encoder contro-control via a signal channel which has a recording unit which registers the connection of the decoder.

The signal channel comprises a telephone connection, and the receiver has components for automatic establishment of telephonic connection at a specific time, together with devices for permanent storage of the data as received within a predetermined successive time interval. (Provisional Basic advised week E22)

1/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003046150
WPI Acc No: 1981-E6178D/198120
Truck bolster ring renewal frame - has cutting and welding torches on moving arm with centring mandrel
Patent Assignee: WEAR C W (WEAR-I)

Inventor: **CARL R J**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 4264058	A	19810428				198120	B

Priority Applications (No Type Date): US 80112943 A 19800117

Abstract (Basic): US 4264058 A

For cutting the worn bolster ring from a truck bolster and for welding a new ring onto the truck bolster a clamp is pivotally mounted on a frame and centres the bolster and clamps it. A hydraulic cylinder pivotally moves the clamp from a horizontal position to a vertical position. A cutting torch on a horizontally movable arm is moved in place adjacent the bolster ring.

After the worn ring has been cut, the torch is removed from the arm, with a ring mandrel installed. A new bolster ring is positioned on the mandrel and adjacent the truck bolster. The ring is tack welded and the horizontal arm retracted. The mandrel is removed from the horizontal arm and a welding torch is installed.

SYSTEM:OS - DIALOG OneSearch
File 350:Derwent WPIX 1963-2001/UD,UM &UP=200201
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*File 350: Price changes as of 1/1/02. Please see HELP RATES 350.
More updates in 2002. Please see HELP NEWS 350.
File 347:JAPIO OCT 1976-2001/Aug(UPDATED 011203)
(c) 2001 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run. See HELP NEWS 347 for details.

Set	Items	Description
S1	96723	SILICON(W)OXIDE OR SI(W)OXIDE OR SIO OR (OXOSILYLENE(W)28SI) OR (SILICON (N) MONOXIDE) OR (SILICON(2N) MONOXIDE)
S2	96723	SILICON(W)OXIDE OR SI(W)OXIDE OR SIO OR (OXOSILYLENE(W)28S-I) OR (SILICON(2N) MONOXIDE)
S3	45827	SILICON(W)NITRIDE OR SI(W)NITRIDE OR SIN OR (SILICON(2N) M-ONONITRIDE)
S4	2921	(SILICON (N)NITRIDE(N) OXIDE) OR (SILICON (N)NITRIDE(N) OX-IDE) OR (DISILICON(N) OXYDINITRIDE) OR (DISILICON(N) OXYNITRI-DE) OR (SILICON(N)OXYNITRIDE) OR (SI(N) OXYNITRIDE? ?)
S5	31915	DIAMOND OR (DIAMOND(3N)CARBON)
S6	137	(FLUORIN?(W) DOP?(W) OXIDE?) OR ((FLUORIN?) (2N)(OXIDES))
S7	212	F(W)DOP???
S8	1170	(ANTI(W)FUSE? ?) OR ANTIFUSE? ? OR OTP OR ((ONE)(N)(TIME)(-N)(PROGRAM?))
S9	544204	(DIELECTRIC? OR OXIDE OR INSULAT?)(3N)(FILM? ? OR LAYER? OR COAT???? OR MATERIAL?)
S10	387589	((ANTI(N)REFLECT?)(3N) (COAT???? OR FILM? ? OR LAYER?)) OR ((DICHROIC) (2N)(FILTER? OR MIRROR)) OR (FRESNEL(W)REFLECT?) -OR REFLECT?
S11	141915	(POLYIMIDE? ? OR POLYAMIDE? ? OR PARYLENE OR PARALYENE)
S12	735008	(ALUMINUM OR AL OR TUNGSTEN OR W)
S13	504970	(COPPER OR CU OR CHROMIUM OR CR OR GOLD OR AU)
S14	241006	(PLATINUM OR PT OR PALLADIUM OR PD)
S15	114072	(SELENIUM OR SE OR GERMANIUM OR GE)
S16	349	S6 OR S7
S17	386	S8 AND S9
S18	181	S17 AND (VIA OR VIAS OR TRENCH? OR HOLE? ? OR CHANNEL OR G-ROOVE? OR EDGE? OR FLUSH?)
S19	18	S18 AND (S1 OR S2 OR S5 OR S16)
S20	5	S18 AND (S11 OR POLYMETHYLMETHACRYLATE? OR POLY(W)METHYLME-THACRYLATE?)
S21	666	SILICON(W)OXIDES OR SI(W)OXIDES OR (SILICON (N) MONOXIDES) OR (SILICON(2N) MONOXIDES)
S22	138	SILICON(W)NITRIDES OR SI(W)NITRIDES OR (SILICON(2N) MONONI-TRIDES)
S23	29	(SILICON (N)NITRIDE(N) OXIDES) OR (SILICON (N)NITRIDE(N) O-XIDES) OR (DISILICON(N) OXYDINITRIDES) OR (DISILICON(N) OXYNI-TRIDES) OR (SILICON(N)OXYNITRIDES)
S24	37	S18 AND (S21 OR S22 OR S23 OR S2 OR S3 OR S4 OR CARBON? ? -OR S15 OR ((COMPOUND)(2N)(SEMICONDUCTOR?)) OR S10)
S25	18	S19 NOT S20
S26	0	S25 NOT S24
S27	42	S19 OR S20 OR S24

? T S27/3,AB/1-42

27/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014051202
WPI Acc No: 2001-535415/200159
XRAM Acc No: C01-159410
XRPX Acc No: N01-397542
Fabrication of capacitor used in memory e.g. dynamic random access memory, involves forming bottom electrode and tantalum **oxide film**, introducing nitrogen into tantalum **oxide film** to form tantalum oxynitride film, and forming top electrode
Patent Assignee: AL-SHAREEF H N (ALSH-I); DEBOER S J (DEBO-I); GEALY D (GEAL-I); THAKUR R P S (THAK-I)
Inventor: AL-SHAREEF H N; DEBOER S J; GEALY D; THAKUR R P S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20010011740	A1	20010809	US 9831526	A	19980226	200159	B

Priority Applications (No Type Date): US 9831526 A 19980226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010011740	A1		13	H01L-021/8242	

Abstract (Basic): US 20010011740 A1
Abstract (Basic):

NOVELTY - A capacitor is fabricated on an integrated circuit, by sequentially forming a bottom plate electrode (104), and a tantalum **oxide film** (102). The tantalum **oxide film** is annealed in an environment containing oxygen. Nitrogen is introduced to the tantalum **oxide film** to form a tantalum oxynitride film. A top plate electrode (106) is formed on the tantalum oxynitride film.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(A) a capacitor comprising bottom plate electrode, a tantalum oxynitride film, and a top plate electrode;

(B) a memory comprising a memory array having capacitors, a control circuit which is coupled to the memory array, and address logic which is operatively coupled to the memory array and the control logic; and

(C) a method of operating an **antifuse** comprising applying a voltage across the electrodes of the capacitor, forming a **hole** in the tantalum oxynitride film, and creating 1000-6000 Ohm resistance.

USE - The method is used in the fabrication of capacitors used in a memory array of a memory, e.g. dynamic random access memory.

ADVANTAGE - The method provides capacitors having relatively high capacitance to area ratio. The capacitor is less affected by heat to have a diminished leakage current, and has an enhanced reliability.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional representation of a polysilicon electrode stacked, double-sided capacitor.

27/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014039284

WPI Acc No: 2001-523497/200158
XRAM Acc No: C01-156425
XRPX Acc No: N01-387968

Production of conducting pathways on an integrated chip comprises applying a stacked **dielectric layer**, carrying out photolithography, etching, applying conducting material and removing, and applying an **insulating layer**

Patent Assignee: INFINEON TECHNOLOGIES AG (INFN)
Inventor: LEHR M; LEIBERG W

Number of Countries: 026 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10021098	C1	20010920	DE 1021098	A	20000420	200158	B
EP 1148542	A2	20011024	EP 2001107218	A	20010323	200171	

Abstract (Basic): DE 10021098 C1
Abstract (Basic):

NOVELTY - Production of conducting pathways on an integrated chip comprises:

(i) applying a stacked **dielectric layer**;

(ii) carrying out photolithography to define contact **holes** (30);

(iii) etching the **holes**;

(iv) applying conducting material and removing outside of the **holes**;

(v) applying an **insulating layer** (50);

(vi) carrying out photolithography to define conducting pathways;

(vii) etching conducting pathway **trenches** (80); and

(viii) applying conducting material and removing outside of the **trenches**.

DETAILED DESCRIPTION - Production of conducting pathways on an integrated chip comprises:

(a) applying a stacked **dielectric layer** consisting of a lower (21) and an upper **dielectric layer** (22) with an antireflection layer (60) arranged between them;

(b) carrying out photolithography to define contact **holes** (30) in the **dielectric layer**;

(c) etching the **holes** in the stacked layer;

(d) applying conducting material and removing the material outside of the **holes** so that recesses (40) are formed over the contact **holes**;

(e) applying an **insulating layer** (50);

(f) carrying out photolithography to define conducting pathways in the region of individual contact **holes** on the **insulating layer**;

(g) etching conducting pathway **trenches** (80) in the **insulating layer** and the upper **dielectric layer** lying underneath so that the antireflection layer acts as an etch stop; and

(h) applying conducting material and removing the material outside of the **trenches** and the recesses over the contact **holes**.

Preferred Features: The **insulating layer** is made from **silicon nitride**. The antireflection layer is a light-absorbing inorganic material, especially **silicon oxynitride**.

Polycrystalline silicon is used to fill the contact **holes** and tungsten is used to fill the **trenches** and the recesses above the contact **holes**.

27/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013564905
WPI Acc No: 2001-049112/200106
Related WPI Acc No: 1999-590564; 2001-342401
XRAM Acc No: C01-013428
XRPX Acc No: N01-037598
Capacitor for use in dynamic random access memory, has electrodes with silicon **germanium** and polysilicon layers, which are formed on either sides of **silicon nitride dielectric layers** **via** conductive barrier layers
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: MERCALDI G A; NUTTALL M; THAKUR R P S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6150706	A	20001121	US 9832182	A	19980227	200106	B

Priority Applications (No Type Date): US 9832182 A 19980227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6150706	A		10	H01L-029/00	

Abstract (Basic): US 6150706 A
Abstract (Basic):
NOVELTY - Semiconductive electrode (22) having layers (24a, 24b) made of silicon **germanium** and polysilicon, is formed adjacent to one side of **silicon nitride dielectric layer** (28), **via** a conductive barrier layer (26). Another electrode (32) having hemispherical silicon grain polysilicon and silicon **germanium** layers, is formed on another side of **dielectric layer**, **via** another conductive barrier layer (30).
DETAILED DESCRIPTION - The conductive barrier layer (26) comprises tungsten nitride, tungsten **silicon nitride** and titanium **silicon nitride**

27/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013539120
WPI Acc No: 2001-023326/200103
Related WPI Acc No: 2001-578602
XRAM Acc No: C01-007057
XRPX Acc No: N01-018128
Anti-fuse for enabling or disabling components on a semiconductor integrated circuit has **dielectric layer** between conductive **layers**, well region, and shallower more lightly doped region
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: GRAVELLE R M; SHER J C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6140692	A	20001031	US 97865282	A	19970529	200103	B

Priority Applications (No Type Date): US 97865282 A 19970529
Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes
US 6140692 A 10 H01L-029/00
Abstract (Basic): US 6140692 A
Abstract (Basic):
NOVELTY - An **anti-fuse** formed on a silicon substrate of a first conductivity type comprises a **dielectric layer** between two conductive layers, a well region under a portion of the second conductive layer to which a third conductive layer is contacted, and a shallower more lightly doped region within the well region.
DETAILED DESCRIPTION - An **anti-fuse** (51) formed on a silicon substrate of a first conductivity type, comprises a first conductive layer (58) on the substrate surface, a **dielectric layer**, and a second conductive layer (62) having a portion extending beyond the **dielectric layer** above the substrate surface to which a third conductive layer is contacted. It has a well region (64) in the substrate under the portion of the second conductive layer, and a shallower more lightly doped region (90) within the well region. The well and shallower regions have a second conductivity type.

27/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013465697
WPI Acc No: 2000-637640/200061
XRAM Acc No: C00-191761
XRPX Acc No: N00-472894
Fabrication of **anti-fuse** module and dual damascene interconnect structure involves forming metal line, depositing and patterning **silicon nitride** and fusing element layers, and forming **anti-fuse** metal line and interconnect
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N)
Inventor: CHU S S; LEE C; SHAO K; XU Y
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6124194	A	20000926	US 99439365	A	19991115	200061	B

Abstract (Basic): US 6124194 A
Abstract (Basic):
NOVELTY - An **anti-fuse** module and dual damascene interconnect structure is fabricated by forming a first metal line, depositing and patterning **silicon nitride** layer, depositing and patterning a fusing element layer, and simultaneously forming an **anti-fuse** line and a dual damascene interconnect on and contacting with a second metal line.
DETAILED DESCRIPTION - An **anti-fuse** module and dual damascene interconnect structure is fabricated by forming a first metal **via** within a first **dielectric layer** (20) within an **anti-fuse** area (16) and contacting a first metal line (12); depositing a **silicon nitride** (**SiN**) **layer** on the **dielectric layer** and metal **via** (26); patterning the **SiN** layer (28) to form at least two openings; depositing and patterning a fusing element layer on the patterned **SiN** layered structure to form a fusing element on the metal **via**; and simultaneously forming an **anti-fuse** metal line (56) on the fusing element (44) to form an **anti-fuse** module within the **anti-fuse** area, and a dual damascene interconnect (58) and

contacting with a second metal line and within the interconnect area (18). A first opening exposes the first metal **via** and a second opening exposes a portion of the first **dielectric layer** above the second metal line (14).

27/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013370382
WPI Acc No: 2000-542321/200049
Related WPI Acc No: 1996-433092; 1998-062475; 1998-436562; 1999-204117
XRAM Acc No: C00-161334
XRPX Acc No: N00-401063
Antifuse for an integrated circuit, has metal conductors, **insulating layer**, conductive plug, **dielectric material**, and programmable **material** having amorphous silicon layer
Patent Assignee: QUICKLOGIC CORP (QUIC-N)
Inventor: GORDON K E; WONG R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6097077	A	20000801	US 91691950	A	19910426	200049	B
			US 91698648	A	19910510		
			US 92874983	A	19920423		
			US 92891675	A	19920528		
			US 92892466	A	19920601		

Abstract (Basic): US 6097077 A
Abstract (Basic):
NOVELTY - An **antifuse** includes two metal conductors, an **insulating layer**, a conductive plug, a **dielectric material**, and a programmable material having an amorphous silicon layer.
DETAILED DESCRIPTION - An **antifuse** (510) comprises two metal conductors (26, 27), an **insulating layer** overlying the first conductor and having an opening (544), a conductive plug (545) at least partially filling the opening and contacting the first conductor, a **dielectric material** (540) comprising silicon and nitrogen, and a programmable material overlying the plug and having an amorphous silicon layer (25). The plug extends no higher than the top **edge** of the opening and does not extend outside the opening. The programmable **material insulates** the plug from the second conductor when the **antifuse** is unprogrammed. A conductive path (210) is formed between the plug and second conductor through the programmable material when the **antifuse** is programmed. A bottom surface of the programmable material is in contact with the **dielectric material** top surface above the plug.

27/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013318166
WPI Acc No: 2000-490105/200043
XRAM Acc No: C00-147137
XRPX Acc No: N00-363665
Integrated circuit apparatus for programmable logic chips, comprises

antifuse having conductive interconnect, interlevel dielectrics, conductors, and **via** comprising second conductive interconnect and **trench**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: GAMBINO J P; KIRIHATA T; NARAYAN C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6081021	A	20000627	US 987889	A	19980115	200043	B

Abstract (Basic): US 6081021 A
Abstract (Basic):

NOVELTY - An integrated circuit apparatus comprises a first device comprising a conductive interconnect, interlevel dielectric with an upper surface and an opening, a conductor on the **insulating layer** at the bottom of the opening, a second interlevel dielectric, a second conductor; and a second device comprising a second conductive interconnect and a **trench** in the interlevel dielectric.

DETAILED DESCRIPTION - The integrated circuit apparatus comprises a first device comprising:

(a) a conductive interconnect (310);

(b) interlevel dielectric (305) with an upper surface and an opening (320) that extends through the dielectric to the interconnect where the opening has sidewalls and bottom;

(c) an **insulating layer** (322), a conductor that is planarized to the upper surface of the dielectric;

(d) a second interlevel dielectric (307) which has a second opening (330);

(e) a second conductor (342); and

(f) a second device comprising a second conductive interconnect (315) having a third opening (340), sidewalls, a bottom, a third opening, a third opening depth, and a **trench**.

27/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013110530
WPI Acc No: 2000-282401/200024
Related WPI Acc No: 1999-008890
XRPX Acc No: N00-212540
Field effect transistor for **one-time programmable** nonvolatile memory element during fabrication of very large scale integrated circuit dies on a semiconductor wafer
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: LI W; MA M K F; SOMASEKHARAN R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6040608	A	20000321	US 96652376	A	19960523	200024	B
			US 97964164	A	19971104		

Abstract (Basic): US 6040608 A
Abstract (Basic):

NOVELTY - An n-**channel** metal-oxide-semiconductor field effect transistor on and in a substrate (100) of p-type doping includes a body terminal (110) formed from a heavily doped p+ diffusion region, a

source terminal (115) and a drain terminal (120). A gate terminal (125), preferably of conductively doped polysilicon, is formed on a thin **layer** (130) of **silicon dioxide**. Short drain voltage is applied exceeding the drain-to-source breakdown voltage, to produce a drain source resistance not affected by voltages applied to the gate terminal.

27/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012794182
WPI Acc No: 1999-600411/199951
Related WPI Acc No: 1999-356420
XRAM Acc No: C99-174746
XRPX Acc No: N99-442546
Antifuse interconnect between two conducting layers of a printed circuit board formed by the application of a programming voltage
Patent Assignee: PROLINX LABS CORP (PROL-N)
Inventor: CHIANG S S; LAN J J D; SHEPHERD W H; WU P Y F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5962815	A	19991005	US 95374941	A	19950118	199951	B

Abstract (Basic): US 5962815 A
Abstract (Basic):

NOVELTY - The **antifuse** comprises two conductors separated by a dielectric that comprises a first material with a number of **via holes** filled with a second material whose breakdown voltage is lower than the first material, thus forming a number of **antifuses**.

DETAILED DESCRIPTION - The circuit board structure comprises a **dielectric layer** located between first and second electrodes, wherein the **dielectric layer** is formed of a first non-conductive material which defines a **hole** extending from the first electrode to the second electrode, the **hole** being filled with a second material to form an **antifuse** between the electrodes. The second material includes a polymer and conductive particles, and as a whole is non-conductive. On the application of a programming voltage between the electrodes to breakdown the polymer, the conductive particles forms at least a portion of an electrical conductor connecting the first electrode to the second electrode, wherein the conductive particles have a dimension approx. the diameter of the **hole**.

The first material is photoimagible. The second material has a breakdown voltage less than the breakdown voltage of the first material.

27/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012765213
WPI Acc No: 1999-571340/199948
Related WPI Acc No: 1998-178487
XRAM Acc No: C99-166710
XRPX Acc No: N99-420986
Integrated circuit comprising an amorphous silicon **antifuse**

structure
Patent Assignee: VLSI TECHNOLOGY INC (VLSI-N)
Inventor: MANLEY M H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5962911	A	19991005	US 96639557	A	19960429	199948	B
			US 97941512	A	19970930		

Abstract (Basic): US 5962911 A
Abstract (Basic):

NOVELTY - Dummy metallization and polysilicon features are formed in close proximity to the **antifuse** structure. This results in a thicker **layer** of **dielectric** being formed over the **antifuse** structure so that it is not etched or contaminated during subsequent etching of interconnection **via holes**.

DETAILED DESCRIPTION - Fabrication of an integrated circuit comprising:

(a) Substrate with a number of active, dummy diffusion, and raised field oxide regions (114);

(b) First **dielectric layer** (116) over the substrate with higher regions over the raised field oxide;

(c) First metallization for defining a network of lines at least some of which are arranged to interconnect with preselected active region, and some of which cross over associated field oxide regions;

(d) **Antifuse** (130) positioned over the first dielectric and over an associated dummy diffusion region and not over filed oxide comprising: (i) Portion of the first metallization over the first dielectric, and an intermediate **dielectric layer** covering a segment of the first metallization with a **via** link opening to provide an electrical path with the portion; (ii) Amorphous silicon formed over the intermediate dielectric contacting the first metallization through the **via** opening; (iii) Barrier layer over the amorphous silicon and a second dielectric over the first dielectric and first metallization having a number of **via holes** (241a,241b,241c) some of which are positioned to communicate with segments of the metallization and one of them communicating with the **antifuse**.

USE - Integrated circuit comprising an amorphous silicon **antifuse** structure

ADVANTAGE - The **antifuse** structure is not over-etched or contaminated during the formation of **vias**, preventing voltage variations.

DESCRIPTION OF DRAWING(S) - The drawing shows an **antifuse** structure.

Silicon substrate (112)
Field oxide (114)
Silicon oxide dielectric (116)
Barrier layer (124)
High density plasma oxide second dielectric (125)
Antifuse structure (130)
Spin on glass layer (132)
High density plasma oxide (135)
Etching material (138)
Via holes (241a,241b,241c)
pp; 10 DwgNo 2H/2

27/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012611522
WPI Acc No: 1999-417626/199935
Related WPI Acc No: 1996-341674; 1996-505643; 1998-192883; 1998-520320; 1998-541532; 1999-008896
XRAM Acc No: C99-122590
XRPX Acc No: N99-311676
Structure for field programmable logic structures
Patent Assignee: PROLINX LABS CORP (PROL-N)
Inventor: CHIANG S S; LAN J J D; NATHAN R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5917229	A	19990629	US 94194110	A	19940208	199935	B
			US 96688241	A	19960729		

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5917229	A		40	H01L-029/00	Cont of application US 94194110

Abstract (Basic): US 5917229 A
Abstract (Basic):
NOVELTY - The fuse is electrically coupled between the second trace and the first trace and has a separable portion formed of at least a second electrically conducting material which has a second melting point lower than a first melting point of the first electrically conducting material so that the separable portion disintegrates on passage of a programming current of a predetermined magnitude for a predetermined duration through the fuse.
DETAILED DESCRIPTION - A structure comprises
(i) a first trace formed as part of a first conductive layer including a first electrically conducting material;
(ii) a second trace formed as part of a second conductive layer;
(iii) an **insulating** plastic **material** between the traces; and
(iv) an electric fuse formed as a portion of an inner conductive layer of the structure.
The fuse is electrically coupled between the second trace and the first trace and has a separable portion formed of at least a second electrically conducting material which has a second melting point lower than a first melting point of the first electrically conducting material so that the separable portion disintegrates on passage of a programming current of a predetermined magnitude for a predetermined duration through the fuse. The second melting point is lower than 1000 degrees C. The separable portion of the fuse comprises an electrically conductive trace having a **hole**.

27/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012550314
WPI Acc No: 1999-356420/199930
Related WPI Acc No: 1999-600411
XRAM Acc No: C99-105372
XRPX Acc No: N99-265254
Antifuses used as programmable interconnect in printed circuit

board and multichip module substrate
Patent Assignee: PROLINX LABS CORP (PROL-N)
Inventor: CHIANG S S; LAN J J D; SHEPHERD W H; WU P Y F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5906043	A	19990525	US 95374941	A	19950118	199930	B
			US 97884823	A	19970630		

Priority Applications (No Type Date): US 95374941 A 19950118; US 97884823 A 19970630
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5906043	A		14	H01K-003/10	Div ex application US 95374941

Abstract (Basic): US 5906043 A
Abstract (Basic):

NOVELTY - In a site of a PCB that needs a **via**, an **antifuse** is fabricated and the **antifuse** is programmed to form an electrical conductor.

DETAILED DESCRIPTION - Preparing a printed circuit board, comprises:

(a) applying a first **dielectric material** on a first conductive **layer**; the first **dielectric material** including a printed circuit board **dielectric material**;

(b) forming a number of **holes** at predetermined locations in the first **dielectric material**; each location being for forming an electrical conductor;

(c) filling the **holes** with a material including a polymer and conductive particles (90A,90B,90C) to form a compound layer;

(d) applying a second conductive layer on the compound layer by electroless copper deposition, electrolytic copper deposition or laminating;

(e) etching the first conductive layer to form a first electrode (221); and

(f) etching the second conductive layer to form a second electrode (222).

USE - Formation of an electrical conductor between two electrodes of a PCB by applying a programming voltage across a **dielectric layer** that separates the two electrodes. **Antifuses** used as programmable interconnect in substrates other than silicon, such as printed circuit board and multichip module substrate (MCM). For flex circuits, PCMCIA cards.

27/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012520150
WPI Acc No: 1999-326256/199927
XRAM Acc No: C99-096372
XRPX Acc No: N99-244739
Forming programmable **antifuses** in integrated circuit
Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: THOMAS M E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5904507	A	19990518	US 9828190	A	19980223	199927	B

Abstract (Basic): US 5904507 A
Abstract (Basic):
NOVELTY - A method for a programmable **antifuse** in an IC comprises forming a **via** (210) in an **insulating layer** (204) on a substrate and field, depositing an interlayer (212) and a conductive **layer** (214) over the **insulating layer** and **via** sidewalls, etching these (212,214) to isolate an **antifuse** within the **via** and depositing a second conductor within the **via**.

27/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012506166
WPI Acc No: 1999-312271/199926
XRAM Acc No: C99-092145
XRPX Acc No: N99-233206
Integrated circuit including a self-aligned **antifuse**
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: KWOK S P; WRIGHT P J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5903042	A	19990511	US 9620342	A	19960619	199926	B
			US 97873943	A	19970612		

Abstract (Basic): US 5903042 A
Abstract (Basic):
NOVELTY - An **antifuse** base is formed over the interconnect **layer** before the interlevel **dielectric** is formed. A **via** is formed thorough the dielectric aligned with the base and then the **antifuse** structure formed over the **via**. The advantage of having the base self-aligned to the first interconnect layer is that the alignment tolerances are increased, thus easing manufacture, while maintaining low capacitance interconnect and increased reliability.
DETAILED DESCRIPTION - **Antifuse** comprising; (a) First interconnect layer. (b) Layer of titanium - tungsten barrier metal self-aligned in one dimension to the first interconnect layer and covering only a portion of it. (c) Amorphous silicon **antifuse** dielectric over the barrier metal. (d) Second interconnect over the dielectric

27/3,AB/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012506165
WPI Acc No: 1999-312270/199926
XRAM Acc No: C99-092144
XRPX Acc No: N99-233205
Integrated circuit device with fuse-**antifuse** structures
Patent Assignee: APTIX CORP (APTI-N)
Inventor: COMER A E; GRAHAM S; LA FLEUR M D; LEE Y; LIU C; WHITTEN R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5903041	A	19990511	US 94263920	A	19940621	199926	B

Abstract (Basic): US 5903041 A
Abstract (Basic):
NOVELTY - Integrated circuit device has a first and a second metallization layer separated by a two-**layered dielectric**. A second metallization **layer** is located above the first metallization layer and a B-fuse structure or an AB-fuse structure is disposed between the metallization layers
DETAILED DESCRIPTION - An integrated circuit device has a first and a second metallization **layer** separated by a **dielectric** comprising a first **dielectric layer** and a second **dielectric layer** over the first **dielectric layer**. A second metallization layer is located above the first metallization layer and a B-fuse structure is disposed between the metallization layers.
The B-fuse comprises:
(i) a first **via** opening in the first **dielectric layer** which penetrates the first **dielectric layer** to provide electrical access to the first metallization layer;
(ii) a fuse material **layer** over the first **dielectric layer** and in the first **via** opening, which is in electrical contact with the first metallization layer and includes a necked portion, vertically adjacent an air gap, configured to blow upon application of a predetermined current across the necked portion;
(iii) a second **via** opening in the second **dielectric layer** which penetrates the second **dielectric layer** to contact the fuse material layer; and
(iv) an electrically conductive material in the second **via** opening forming a conductive path from the second metallization layer to the fuse material layer.
The second **dielectric layer** includes at least1 sacrificial **via** opening and is covered with a passivation layer of **polyimide** material which seals the sacrificial **via** opening.

27/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012398010
WPI Acc No: 1999-204117/199917
Related WPI Acc No: 1996-433092; 1998-062475; 1998-436562; 2000-542321
XRAM Acc No: C99-059415
XRPX Acc No: N99-150320
Antifuse for programmable ROM, logic devices or gate arrays
Patent Assignee: QUICKLOGIC CORP (QUIC-N)
Inventor: GORDON K E; WONG R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5880512	A	19990309	US 91691950	A	19910426	199917	B
			US 91698648	A	19910510		
			US 92874983	A	19920423		
			US 92891675	A	19920528		
			US 92892466	A	19920601		
			US 96651102	A	19960521		
			US 96768601	A	19961218		

Abstract (Basic): US 5880512 A

Abstract (Basic):
NOVELTY - **Antifuse** structure has amorphous silicon within an opening in **insulative layer**, surrounded by two metallic conductive layers which are separated by a dielectric spacer.
DETAILED DESCRIPTION - **Antifuse** structure has an **insulating layer** (20) on a metal conductor (18). The insulator has an opening (22), with a programmable material (25) in it. This material is nonconductive when the **antifuse** is unprogrammed, and forms a conductive path when programmed. A second metal conductor (26, 27) lies over and contacts the programmable material. A sidewall spacer (320a,b) in the opening separates the conductors.
Preferred Features: The programmable material is amorphous material, and the spacer is a dielectric, preferably **silicon dioxide**. The second conductor comprises aluminum (27), with a titanium-tungsten barrier (26) preventing the conductive material from spiking into the programmable material. When the structure is programmed, material surrounding the conductive path and the path itself have linear thermal expansion coefficients (LTCE) at 25degreesC within 4 times of each other.

27/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012103241
WPI Acc No: 1998-520153/199844
XRAM Acc No: C98-156146
XRPX Acc No: N98-406251
One-time fusible link for field programmable gate arrays - using an amorphous silicon@ **antifuse** layer with a barrier layer to protect it in subsequent processing
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: CHANG T
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5807786	A	19980915	US 97902754	A	19970730	199844	B

Abstract (Basic): US 5807786 A
An **antifuse** structure based on an interconnect is formed by; (a) Forming an interconnect structure of Al alloy (1) contacting active elements on a substrate and depositing an **insulator layer** of **silicon oxide** (2) over it. (b) Forming a **via hole** (3) in the insulator to expose the interconnect. (c) Forming sidewall spacers of TiN (4) on the inside walls of the **via hole**, then filling it with a tungsten metal plug (5b), and filling recesses in the plug and spacers with **silicon oxide** insulator (6). (d) Forming an amorphous silicon (7) **antifuse** layer contacting the plug with a TiN protective layer (8) and then a second interconnect structure over the **antifuse layer** (10a). The **insulator** fill (6) is planarised to give a smooth surface for the **antifuse** layer

27/3,AB/18 (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011973836
WPI Acc No: 1998-390746/199834

XRPX Acc No: N98-304899
Planar **antifuse** element manufacturing method for FPGA - involves forming wiring electrode contacting **insulating film** which is formed on surface of exposed silicon **germanium** pattern
Patent Assignee: KOREA ELECTRONIC COMMUNICATION (KOEL-N); KOREA ELECTRONICS & TELECOM RES INST (KOEL-N); KOREA ELECTRONICS & TELECOM RES (KOEL-N)
Inventor: CHO K; KIM C; PAEK C; SONG Y; YUN S; BAEK J T; CHO G I; KIM J D; SONG Y H; YOON S J
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10050842	A	19980220	JP 96333983	A	19961213	199834	B
KR 97054316	A	19970731	KR 9549253	A	19951213	199911	
KR 216544	B1	19990816	KR 9549253	A	19951213	200104	

Abstract (Basic): JP 10050842 A
The method involves forming a first **insulating film** (22) and a silicon **germanium** layer (23a) on a semiconductor substrate (21). The silicon **germanium** layer is doped by depositing impurity ions. The doped layer (23b) is patternized to form a silicon **germanium** pattern (23). A second **insulating film** (24) is formed on the first **insulating film**.
A pair of predefined areas of the second **insulating film** are etched to form two contact **holes** (30,31) by which the pattern is exposed. A third **insulating film** (25) is formed on the surface of the exposed pattern. A wiring electrode (27) is formed contacting the third **insulating film**.
ADVANTAGE - Reduces loss of input energy for drive of **antifuse** element. Simplifies flattening regulation of **insulating film**. Reduces programming voltag

27/3,AB/19 (Item 19 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011645567
WPI Acc No: 1998-062475/199806
Related WPI Acc No: 1996-433092; 1998-436562; 1999-204117; 2000-542321
XRPX Acc No: N98-049177
Integrated structure with **anti-fuse** for programmable integrated circuit - has layer of programmable material on plug, providing conductive path contacting plug when **anti-fuse** is programmed
Patent Assignee: QUICKLOGIC CORP (QUIC-N)
Inventor: GORDON K E; WONG R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5701027	A	19971223	US 91691950	A	19910426	199806	B
			US 91698648	A	19910510		
			US 92874983	A	19920423		
			US 92891675	A	19920528		
			US 92892466	A	19920601		
			US 96651102	A	19960521		

Abstract (Basic): US 5701027 A
The **antifuse** (510) permanently connects two terminals when sufficient overvoltage is applied. It may be made e.g. of amorphous silicon which becomes conductive polysilicon and is a field

programmable gate array. The **antifuse** includes a metal conductor (538). An **insulating dielectric layer** (540), e.g. **silicon dioxide**, overlays the conductor and has an opening which is occupied by a tungsten plug (545) contacting the conductor.

A filament (210) lies in the **antifuse via** (544). The top surface of the **insulating layer** is coplanar with the top surface of the plug. An amorphous silicon body (25) overlays and contacts the plug and the adjacent portion of the **insulating layer**. The second metal conductor layers (26,27) overlay and contact the amorphous silicon.

27/3,AB/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011153888
WPI Acc No: 1997-131812/199712
Related WPI Acc No: 1998-086264
XRAM Acc No: C97-042520
XRPX Acc No: N97-108878
Dual damascene **anti-fuse** structure mfr. with reduced cost - including deposition of process control layer over **anti-fuse** structure and etching of opening in process control layer, etc.
Patent Assignee: CHARTERED SEMICONDUCTOR MFG LTD PTE (CHAR-N); CHARTERED SEMICONDUCTOR MFG PTE LTD (CHAR-N)
Inventor: CHAN L; ZHENG J Z; ZHENG J
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5602053	A	19970211	US 96628068	A	19960408	199712	B
SG 52951	A1	19980928	SG 971108	A	19970408	199904	

Abstract (Basic): US 5602053 A

Mfr. of an **antifuse** structure comprises: (a) providing a 1st conductive layer; (b) depositing a 1st **insulating layer** on the 1st conductive layer; (c) patterning and etching the 1st **insulating layer** to form a **trench**; (d) patterning and etching the 1st **insulating layer**, including the **trench** to form a cavity extending from inside the **trench** down to the level of the 1st conductive layer; (e) depositing a barrier **layer** on the 1st **insulating layer** and on all walls of the **trench** and the cavity; (f) depositing a 2nd conductive layer so as to more than fill the cavity and the **trench**; (g) removing the 2nd conductive layer and the barrier layer as far as the level of the 1st **insulating layer** to form a 1st dual damascene connector (DDC) having an upper surface; (h) depositing a 1st layer of **Si nitride** on the **antifuse** structure; (i) depositing a 1st layer of amorphous Si on the nitride layer; (j) depositing a 2nd layer of **Si nitride** on the 1st layer of amorphous Si; (k) depositing a 2nd layer of amorphous Si on the 2nd layer of nitride; (l) patterning and then etching the 1st and 2nd layers of **Si nitride** and amorphous Si to form a pedestal that overlaps the 1st DDC; (m) depositing a 2nd **insulating layer** on the 1st **insulating layer** and on the 2nd layer of amorphous Si; and (n) forming a 2nd DDC that extends through the 2nd **insulating layer** down to and making electrical contact with the 2nd layer of amorphous Si.

27/3,AB/21 (Item 21 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011115182
WPI Acc No: 1997-093107/199709
XRAM Acc No: C97-029915
XRPX Acc No: N97-076987
Semiconductor device with **anti-fuse** element mfr. for e.g. semiconductor IC - involves forming second aluminium@ wiring on whole surface of curing film including in contact **holes** and contacts directly with first aluminium@ wiring exposed under first contact **hole**
Patent Assignee: NEC YAMAGATA LTD (NIDE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8330530	A	19961213	JP 95133672	A	19950531	199709	B

Abstract (Basic): JP 8330530 A
The mfg method involves forming a first **insulating film** (2) on surface of a semiconductor substrate (1). A pair of first Al wiring patterns (10-1,10-2) are selectively formed on the first **insulating film**. A **silicon nitride** film (11) is formed on whole surface of first **insulating film** by hiding the wiring pattern. A curing film (12) is then formed with planarised upper surface on this **silicon nitride** film. A contact **hole** (5-1B) is then formed corresponding to the wiring patterns.
A heat treatment is performed such that water content and organic solvent present in the curing film gets evaporated from exposing portion of the wiring patterns under the contact **holes**. A third **insulating film** (13) is thus formed at the bottom portion of first contact **hole**. This third **insulating film** acts as the **anti-fuse** element. A second Al wiring (14) which acts as the **anti-fuse** element is formed on whole upper surface of curing film including in contact **holes**. The second Al wiring connects with second wiring pattern of first pair directly but with first wiring pattern of first pair indirectly through the third **insulating film**.

27/3,AB/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011108813
WPI Acc No: 1997-086738/199708
Related WPI Acc No: 1998-446251
XRAM Acc No: C97-028182
XRPX Acc No: N97-071495
User-programmable **anti-fuse** with improved **anti-fuse** material - stable below 600 deg.C, with low defect density, low breakdown field and low moisture content
Patent Assignee: ACTEL CORP (ACTE-N)
Inventor: ELTOUKHY A A; GO Y; MCCOLLUM J L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5592016	A	19970107	US 95423518	A	19950414	199708	B

Abstract (Basic): US 5592016 A

An **antifuse** comprises (a) a first electrode; (b) an **antifuse** layer over the first electrode which comprises a solid **hydrocarbon** material stable at temps. below 600 deg. C, having a defect density less than 100 defects/cm2, a breakdown field less than 10 MV/cm, a dielectric constant lower than 4.0 and a resistivity greater than 104 Omega cm; and (c) a second conductive electrode over the **antifuse** layer.

Also claimed are (i) an **antifuse** with an interlayer dielectric over the first electrode and having an **antifuse via**, the **antifuse** material is formed in the **antifuse via**; (ii) an **antifuse** which further comprises a conductive plug in the **antifuse via** and planarised with the upper surface of the interlayer **dielectric**, the **antifuse layer** being disposed over the conductive plug; (iii) an **antifuse** comprising (a) a first conductive electrode, (b) a barrier layer disposed over the first conductive electrode, (c) an **antifuse** layer disposed over the barrier **layer**, (d) an interlayer **dielectric** formed over the **antifuse** layer and contg. an **antifuse via**, (e) a conductive plug in the **antifuse via** and in contact with the **antifuse** layer, and (f) a second conductive electrode disposed over the conductive plug; (iv) an **antifuse** which further comprises a second barrier layer disposed over the **antifuse** layer and in contact with the interlayer dielectric; (v) an **antifuse** comprising (a) a first electrode, (b) an interlayer dielectric over the first **antifuse** electrode and having an **antifuse via** formed, (c) a conductive plug in the **antifuse via** and planarised with an upper surface of the interlayer dielectric, (d) spaced-apart pads in the upper surface of the interlayer dielectric and having a thickness of 100-1,500 Angstrom , (e) an **antifuse** layer over the conductive plug and of equal thickness to the spaced-apart pads, and (f) a second electrode over the **antifuse** layer; and (vi) an **antifuse** in which the **antifuse** layer comprises a spun-on layer of the solid **hydrocarbon** material.

27/3,AB/23 (Item 23 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011074720
WPI Acc No: 1997-052644/199705
Related WPI Acc No: 1991-305095; 1992-152620; 1993-413420; 1995-089373; 1995-146897; 1996-370725; 1996-412168; 1997-020510; 1997-234689; 1997-479573; 1998-347523; 1998-376940; 1998-413074
XRPX Acc No: N97-043136
Double half **via anti-fuse** - comprises layers of **anti-fuse material** and **dielectric material** between upper and lower electrodes communicating **via** aligned **holes** in **dielectric layers**
Patent Assignee: ACTEL CORP (ACTE-N)
Inventor: MCCOLLUM J L
Number of Countries: 021 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9641374	A1	19961219	WO 96US7989	A	19960529	199705	B
EP 835525	A1	19980415	EP 96916763	A	19960529	199819	
			WO 96US7989	A	19960529		

US 5866937	A	19990202	US 90508306	A	19900412	199912	
			US 90604779	A	19901026		
			US 934912	A	19930119		
			US 94231634	A	19940422		
			US 95482270	A	19950607		

Abstract (Basic): WO 9641374 A

The device includes a planar conductive lower electrode(14) is covered by a layer of **silicon nitride** covered by a layer of amorphous silicon(16). A **dielectric layer**(18) with a **hole** is then deposited.

A layer of **silicon nitride** (22) is deposited over the **dielectric layer** into the **hole**. A conductive upper electrode (20) e.g. titanium nitride, is then deposited covered by a **dielectric layer** (22) with another **hole** aligned with the first. An overlying metal layer (24) is then deposited over the **dielectric layer** (22) and in the **hole** making electric contact with the upper electrode.

ADVANTAGE - Has lower sensitivity to etch selectivity during **antifuse via** etching process. Has improved BVG control.

27/3,AB/24 (Item 24 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010936142
WPI Acc No: 1996-433092/199643
Related WPI Acc No: 1998-062475; 1998-436562; 1999-204117; 2000-542321
XRPX Acc No: N96-364943

Anti-fuse gate array with programmable interconnect structure for producing short circuit - has dielectric spacers covering corners of amorphous silicon@ with planar bottom surface and tungsten plug bridging insulating **via**

Patent Assignee: QUICKLOGIC CORP (QUIC-N)
Inventor: GORDON K E; WONG R J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5557136	A	19960917	US 91691950	A	19910426	199643	B
			US 91698648	A	19910510		
			US 92874983	A	19920423		
			US 92891675	A	19920528		
			US 92892466	A	19920601		

Abstract (Basic): US 5557136 A

The **antifuse** (510) permanently connects two terminals when sufficient overvoltage is applied. It may be made e.g. of amorphous silicon which becomes conductive polysilicon and is a field programmable gate array. The **antifuse** includes a metal conductor (538). An **insulating dielectric layer** (540), e.g. **silicon dioxide**, overlays the conductor and has an opening which is occupied by a tungsten plug (545) contacting the conductor.

A filament (210) lies in the **antifuse via** (544). The top surface of the **insulating layer** is coplanar with the top surface of the plug. An amorphous silicon body (25) overlays and contacts the plug and the adjacent portion of the **insulating layer**. The second metal conductor layers (26,27) overlay and contact the amorphous silicon.

27/3,AB/25 (Item 25 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010770952
WPI Acc No: 1996-267906/199627
Related WPI Acc No: 1995-026285
XRAM Acc No: C96-085121
XRPX Acc No: N96-225230
Semiconductor device with **anti-fuse** elements - useful as low voltage-responsive programmable elements
Patent Assignee: KAWASAKI STEEL CORP (KAWI)
Inventor: KAIZUKA T; OHTA T; SHINRIKI H
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5521423	A	19960528	US 94228257	A	19940415	199627	B
JP 6302701	A	19941028	JP 9390319	A	19930419	199627	
JP 6302700	A	19941028	JP 9390318	A	19930419	199627	

Abstract (Basic): US 5521423 A
A semiconductor device has several **anti-fuse** elements, each having an interlayer **insulating layer** formed between first and second metal wirings, a connection **hole** formed through this **layer** and a **dielectric film** of Ti, Ta, Nb, Zr, Y or Hf oxide formed in the connection **hole** for insulation between the wirings, an intermediate **insulating film** being formed between and in direct contact with the first metal wiring and the **dielectric film** at a region in which direct tunnel conduction is dominant.
Also claimed are (i) a similar device, in which the intermediate **insulating film** is omitted and in which the **dielectric film** comprises a silicon film formed on the first metal wiring, an **insulative silicon oxide film** formed over the silicon film and a lamination film of Ti, Ta, Nb, Zr, Y, Hf or Al oxide formed over the **silicon oxide film**, and (ii) a semiconductor device, in which each **anti-fuse** element comprises (a) a smoothed interlayer **insulating layer** formed between first and second metal wirings; (b) a smoothed connection **hole** formed through this layer; (c) a conductive plug, selected from W, Al and Cu metals, Ti, Ta, Nb, Zr and Hf nitrides and Ti, Ta, Nb, Zr, Y and Hf silicides, filling the connection **hole**; and (d) a planar **dielectric film** of Ti, Ta, Nb, Zr, Y or Hf oxide, covering the interlayer **insulating layer** and the conductive plug for insulation between the conductive plug and the second metal wiring.

27/3,AB/26 (Item 26 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010194253
WPI Acc No: 1995-095507/199513
XRAM Acc No: C95-043860
XRPX Acc No: N95-075296
Mfr of a field programmable gate array - involves formation of **antifuse** layer consisting of **silicon nitride** with a specified nitrogen/silicon composition ratio
Patent Assignee: TOSHIBA KK (TOKE); TOSHIBA MICROELECTRONICS KK (TOSZ)

Inventor: HAMA K; TAKAGI M; YOSHII I; IKEDA N; YASUDA H
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7022513	A	19950124	JP 93190949	A	19930705	199513	B
US 5550400	A	19960827	US 94270458	A	19940705	199640	
CN 1107255	A	19950823	CN 94108287	A	19940705	199732	
US 5866938	A	19990202	US 94270458	A	19940705	199912	
			US 96698349	A	19960815		

Abstract (Basic): JP 7022513 A

The semiconductor device mfg method forms an **insulating film** (4) which covers aluminium wiring layer (2) formed on a substrate. An open **hole** part (5) of tapered shape is formed on this **insulating film**. Ti/TiN barrier metal layer (17) is formed on the first aluminium wiring exposed through the **hole** part. This barrier metal layer acts as the first electrode of an **anti fuse** element. The first electrode and the first aluminium wiring are connected electrically.

An **antifuse** layer (20) consisting of **silicon nitride** is formed on the barrier metal layer. On the top of this **antifuse** layer, a barrier layer (18) which becomes second electrode, is formed. This second electrode and the second aluminium wiring (11) are connected electrically.

27/3,AB/27 (Item 27 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010188120
WPI Acc No: 1995-089373/199512
Related WPI Acc No: 1991-305095; 1992-152620; 1993-413420; 1995-146897; 1996-370725; 1996-412168; 1997-020510; 1997-052644; 1997-234689; 1997-479573; 1998-347523; 1998-376940; 1998-413074
XRPX Acc No: N95-070646
Integrated circuit metal-to-metal **antifuse** structure - has **antifuse** material layer between two multilayer metal interconnect layers
Patent Assignee: ACTEL CORP (ACTE-N)
Inventor: FOROUHI A R; HAMDY E Z; HU C; MCCOLLUM J L
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5387812	A	19950207	US 90508306	A	19900412	199512	B
			US 90604779	A	19901026		
			US 91743261	A	19910809		
			US 92947275	A	19920918		

Div ex patent US 5272101

Abstract (Basic): US 5387812 A
The **antifuse** has a double layer metal interconnect structure. A lower electrode is a first multilayer metal **layer** interconnect on an **insulator**. An inter-metal dielectric on the first metal layer interconnect has an **antifuse via**.
There is **antifuse** material layer of **silicon nitride** in the **via**. An upper electrode is a second multilayer metal layer interconnect.
ADVANTAGE - Avoids **antifuse** material layer stress around cell opening; compatible with **via** plug and sputter deposition processes.

27/3,AB/28 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010159206
WPI Acc No: 1995-060458/199508
Related WPI Acc No: 1993-068855; 1994-120211; 1996-286503; 1997-234689; 1998-347523; 1998-413074
XRPX Acc No: N95-048070
Integrated circuit metal-to-metal **antifuse** with increased predictability breakdown or programming voltage - uses nitride-amorphous **silicon@-nitride** as **antifuse insulating layer**, with titanium silicide **via** contact metallisation, formed by reaction of titanium@ and amorphous silicon@ on insulator
Patent Assignee: ACTEL CORP (ACTE-N); CHEN W (CHEN-I); CHIANG S S (CHIA-I); HAWLEY F W (HAWL-I)
Inventor: CHEN W; CHIANG S S; HAWLEY F W
Number of Countries: 006 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5381035	A	19950110	US 92950264	A	19920923	199508	B
			US 93172132	A	19931221		

Abstract (Basic): US 5381035 A

The **antifuse** has planar layers of nitride, a-Si, a second nitride, and a second a-Si overlaid on a first metallization **layer**. There is a **dielectric layer** on top of the second a-Si layer. There is a **via** completely penetrating the **dielectric layer** and partially penetrating the amorphous silicon layer. A titanium layer over the **via** is thermally reacted with the remainder of the second a-Si layer to form an electrically conductive titanium silicide region in the area of the **via** the thickness of the second a-Si layer. The reaction is self-limiting and stops at the second nitride layer.

There is a second metallization layer over the **via**. The partially etched second a-Si layer forms a part of the second metallization layer.

27/3,AB/29 (Item 29 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009840355
WPI Acc No: 1994-120211/199415
Related WPI Acc No: 1991-305095; 1992-152620; 1993-008597; 1993-068855; 1993-413420; 1995-060458; 1995-089373; 1995-146897; 1996-286503; 1996-362069; 1996-370725; 1996-412168; 1997-020510; 1997-234689; 1997-297373; 1997-479573; 1998-347523; 1998-376940; 1998-413074
XRPX Acc No: N94-094163
Antifuse structure interlayer dielectric for minimal damage to **antifuse** film in **antifuse via** or contact **via** etching - is multilayer sandwich of etch stop dielectric e.g **silicon nitride** on **antifuse** electrode barrier layer or **antifuse** material **layer**, and thicker isolation **dielectric** e.g. **silicon dioxide**, selectively etchable w.r.t. etch stop layer
Patent Assignee: ACTEL CORP (ACTE-N)
Inventor: HAWLEY F W
Number of Countries: 006 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 592078	A1	19940413	EP 93305751	A	19930721	199415	B
JP 6224304	A	19940812	JP 93247539	A	19930908	199437	
US 5464790	A	19951107	US 92950264	A	19920923	199550	
			US 94197102	A	19940215		
			US 94282145	A	19940728		

Abstract (Equivalent): US 5464790 A

The process for fabricating an **antifuse via** comprising the steps of:

forming a first etch-stop **dielectric layer** from a first **dielectric material** over an underlying layer;

forming an isolation **dielectric layer** from a second **dielectric material** over said first etch-stop **dielectric layer**;

etching an **antifuse via** through said isolation **dielectric layer** with an etching process having a selectivity between said first and second **dielectric materials**, performing an over-etch process of from about 30-70% using said first etch-stop **dielectric layer** as an etch stop; and

etching said **antifuse via** through said first etch-stop **dielectric layer** with an etching process having a selectivity between said second **dielectric material** and said underlying layer, performing an over-etch process of from about 30-70% using said underlying layer as an etch stop.

27/3,AB/30 (Item 30 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009366810
WPI Acc No: 1993-060289/199308
XRPX Acc No: N93-046040
One-time, voltage-programmable, read-only memory array - has memory cell IGFET(s), each coupled to reference voltage line **via anti-fuse** element, forming non-folded bit-line architecture
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: LEE R; LOWREY T A
Number of Countries: 003 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 528417	A2	19930224	EP 92114148	A	19920819	199308	B
US 5241496	A	19930831	US 91746824	A	19910819	199336	
JP 6120440	A	19940428	JP 92265625	A	19920909	199422	N
US 5331196	A	19940719	US 91746824	A	19910819	199428	
			US 93114886	A	19930831		

Abstract (Equivalent): US 5241496 A
The array comprises a semiconductor substrate having a series of parallel, alternating, minimum-pitch field isolation region and active area strips, and a series of parallel, minimum-pitch wordlines overlying and perpendicular to the field isolation region and active area strips. The wordlines are insulated from the active areas by a gate **dielectric layer** and are **dielectrically insulated** on their **edges** and upper surfaces. The array further comprises source/drain junction regions between each wordline pair and field isolation strip pair, and a reference voltage line between and coextensive with every other wordline pair that makes anti-fusible contact to each subjacent pair of cell junctions along its length.
Antifusible contact for each cell is made within a **trench** that extends below junction depth, and is lined with conformal **silicon nitride dielectric layer** that breaks down when subjected to a programming voltage. A series of minimum pitch bitlines, which run parallel to the wordlines, completes the memory array. Each bitline makes direct contact with each pair of cell junctions along its length.

27/3,AB/31 (Item 31 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009222052
WPI Acc No: 1992-349475/199242
XRAM Acc No: C92-155169
XRPX Acc No: N92-266616
Improved **antifuses** in an integrated circuit device - using reduced contamination amorphous silicon@ deposition and the replacement of platinum

Patent Assignee: CROSSPOINT SOLUTIONS INC (CROS-N)
Inventor: DIXIT P; HOLZWORTH M R; INGRAM W P; KLEIN R
Number of Countries: 017 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9216976	A1	19921001	WO 92US1995	A	19920312	199242	B
US 5322812	A	19940621	US 91672501	A	19910320	199424	
			US 91782837	A	19911024		

Abstract (Equivalent): US 5670419 A

Fabricating **antifuses** in an integrated circuit comprises depositing a layer of amorphous silicon, the improvement comprising depositing the amorphous silicon layer in a process chamber having a low-pressure atmosphere with essentially no nitrogen, the atmosphere lower than ambient; removing the atmosphere from the chamber at a rate of no more than 2 millitorr per minute; whereby the avoidance of **silicon nitride** deposition in the amorphous silicon layer is enhanced.

Dwg.1h/4

US 5527745 A

In a method of fabricating **antifuses** in an integrated circuit including the steps of forming contact **holes** in an **oxide layer** over a conducting layer of silicon to expose the silicon layer in the contact **holes**, etching the exposed silicon layer by sputtering prior to the deposition of a noble metal, an improvement comprising forming the contact **holes** in the **oxide layer** by etching sidewalls of the contact **holes** as vertically as possible whereby resputtering oxide from the sidewalls to contaminate the silicon layer is avoided in the sputter etching step.

27/3,AB/32 (Item 32 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009083701
WPI Acc No: 1992-211118/199226
XRPX Acc No: N94-177919

Non-volatile semiconductor memory, electrically **one-time programmable** - has single **layer** CVD **silicon dioxide insulator** between gate electrode and source diffusion, with lower dielectric breakdown strength than thermal **silicon dioxide** and **silicon nitride** multilayer insulator at drain side

Patent Assignee: SHARP KK (SHAF)
Inventor: SAKIYAMA K; TANAKA K; YAMAUCHI Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 4091469	A	19920324	JP 90206434	A	19900801	199226	B
US 5331181	A	19940719	US 91735807	A	19910725	199428	
			US 9382511	A	19930625		

Abstract (Basic): JP 4091469 A

The non-volatile semiconductor memory includes a substrate having source and drain diffusion regions and a gate electrode, with an **insulating film** on the substrate just below the gate electrode. The insulator has a section over the source diffusion region, adjacent to an **edge** of the gate electrode, with a smaller dielectric breakdown strength than the rest of the **insulating**

film. The **insulating film** is a **layered** film and has a multilayer structure on the drain side and a single-layer film on the source side, which breaks down at a smaller voltage than on the drain side.

A permanent conductive path is established between the gate electrode and the source diffusion region when a preset voltage is applied to break down the single-layer film on the source side, so that data is electrically written only once. Pref. the single-layer source side film is a CVD SiO2 film, and the laminated film on the drain side is formed by sequential deposition of a SiO2 thermal **oxide film**, a **SiN film** and a SiO2 thermal **oxide film**.

27/3,AB/33 (Item 33 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008801082
WPI Acc No: 1991-305094/199142
XRPX Acc No: N91-233718
Anti-fuse elements of low capacitance - has **silicon dioxide** between diffusion and **silicon nitride** layers and encroachment and undercutting to reduce feature size
Patent Assignee: ACTEL CORP (ACTE-N)
Inventor: MCCOLLUM J L
Number of Countries: 015 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 452090	A	19911016	EP 91303115	A	19910409	199142	B
US 5057451	A	19911015	US 90508303	A	19900412	199144	
JP 4226067	A	19920814	JP 91108859	A	19910412	199239	

Abstract (Equivalent): US 5057451 A

The **antifuse** aperture is mfd. by (a) forming an SiO2 layer over an implanted region, (b) forming an Si3N4 pad over the SiO2, (c) exposing the substrate to an oxidising atmos. to form an intermediate SiO2 layer such that its **edges** encroach underneath the **edges** of the Si3N4 pad, and (d) removing the pad. The pad is obtd. by forming a 1st elongate Si3N4 strip over the implanted region, of a width equal to the min. feature size in the process technology used to produce it, and forming a 2nd strip intersecting the 1st at the location desired to create the **antifuse**.

27/3,AB/34 (Item 34 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007929283
WPI Acc No: 1989-194395/198927
Related WPI Acc No: 1987-356800
XRPX Acc No: N89-148666
Electrically-programmable low-impedance **anti-fuse** element - includes electrode comprising diffusion region covered by **dielectric layer** containing second electrode, both electrodes being heavily doped
Patent Assignee: ACTEL CORP (ACTE-N)
Inventor: HAMDY E Z; MCCOLLUM J L; MOHSEN A M; MCCULLUM J L; CHEN S O; CHIANG S S; CHEN S
Number of Countries: 007 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 323078	A	19890705	EP 88311837	A	19881214	198927	B
JP 2003278	A	19900108	JP 88332729	A	19881228	199007	
US 4899205	A	19900206	US 87137935	A	19871228	199012	
US 5134457	A	19920728	US 86861519	A	19860509	199233	
			US 87137935	A	19871228		
			US 90464223	A	19900112		

Abstract (Equivalent): US 5412244 A

The electrically-programmable low-impedance **antifuse** has a capacitor-like structure with very low leakage before programming and a low resistance after programming. The **antifuse** includes a first conductive electrode which may be formed as a diffusion region in a semiconductor substrate or may be formed from a semiconductor material, such as polysilicon, located above and insulated from the substrate. A **dielectric layer** is disposed over the first electrode.

A second electrode is formed over the **dielectric layer** from a semiconductor material such as polysilicon, or a metal having a barrier metal underneath. At least one of the two electrodes of each **antifuse** if highly-doped or implanted with arsenic such that high concentrations of arsenic exist at the interface between the electrode and the **dielectric layer**.

US 4899205 A

The electrically-programmable, low-impedance **anti-fuse** element, includes a p-type semiconductor substrate. An electrode comprises a diffusion region in the substrate. A **dielectric layer** over the diffusion region includes a **silicon dioxide** portion and a **silicon nitride** portion over the **silicon dioxide** portion. There is a second electrode over the **dielectric layer**. At least one of the electrodes is heavily doped or implanted with arsenic such that a high concentration of arsenic atoms exists at the interface between the **dielectric layer** and the electrode. A controlled radius conductive filament in the **dielectric layer** electrically connects the electrodes.

27/3,AB/35 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06570637
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 2000-156415 [JP 2000156415 A]
PUBLISHED: June 06, 2000 (20000606)
INVENTOR(s): TERAI YUKA
APPLICANT(s): MATSUSHITA ELECTRONICS INDUSTRY CORP
APPL. NO.: 10-330915 [JP 98330915]
FILED: November 20, 1998 (19981120)

ABSTRACT

PROBLEM TO BE SOLVED: To remove such an ion-damaged **layer** as a surface **oxide layer**, which is generated in an **antifuse** film, due to a dry etching when the **antifuse** film is opened, and to realize a program voltage having little variations.

SOLUTION: This manufacturing method is a method for manufacturing a semiconductor device of a structure wherein a lower electrode 13, a **silicon nitride** film 141 and an amorphous silicon film 142 constituting an **antifuse** film 14, are deposited on a semiconductor substrate 11 and an **insulating film** 16 covering the electrode 13, and the film 14 is formed on a first **insulating film** 12. The **film** 16 is subjected to dry etching through a resist 17 having an aperture and after a contact **hole** 18 is formed in the resist 17 and the film 16, the resist 17 is removed with an oxygen plasma. Here, by adjusting properly the dry etching at the formation of the **hole** 18 and the power of the oxygen plasma at the removal of the resist, the thickness of a surface **oxide layer** 19 generated in the film 142 is formed in a thickness of about 3 nm or thinner. As a result, the variations in the **dielectric** strength of the **film** 142 when the film 142 is broken are improved.

27/3,AB/36 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05375030
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 08-330530 [JP 8330530 A]
PUBLISHED: December 13, 1996 (19961213)
INVENTOR(s): YAMAZAKI SATOSHI
APPLICANT(s): NEC YAMAGATA LTD [416643] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 07-133672 [JP 95133672]
FILED: May 31, 1995 (19950531)

ABSTRACT

PURPOSE: To obtain a semiconductor device which can use aluminum wiring without complexing the process and has an **anti-fuse** element with improved flatness.

CONSTITUTION: An **insulation film** formed by the application method of, for example, **polyimide** is used as an interlayer **insulation film** on first aluminum wire 10-1 formed on a semiconductor substrate 1, a contact **hole** 5-1B is opened at a desired part of a curing film 12, heat treatment is made for vaporizing water and organic solvent, and at the sane time a third **insulation film** is formed on the first aluminum wiring system 10-1 within a contact **hole** and is used as the **insulation film** of **anti-fuse** element.

27/3,AB/37 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04638787
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 06-310687 [JP 6310687 A]
PUBLISHED: November 04, 1994 (19941104)
INVENTOR(s): JINRIKI HIROSHI
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APPLICANT(s): KAWASAKI STEEL CORP [000125] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-092960 [JP 9392960]
FILED: April 20, 1993 (19930420)

ABSTRACT

PURPOSE: To obtain an **antifuse**, which is not subjected to dielectric breakdown by voltage lower than predetermined voltage, by subjecting a silicon film to vapor phase epitaxy on the irregularity of a metal surface and by laminating an **insulating material** on the silicon **film** to constitute an **insulating film**.

CONSTITUTION: A titanium nitride film is formed as interleaved layer 18 on a metal wiring 11 and an **insulating layer** 14 composed of **silicon oxide** is formed on the titanium nitride film. Then, a connecting **hole** 15 is formed at the predetermined place of the **insulating layer** 14. After that, when monosilane gas is decomposed under a reduced pressure and at a high frequency, amorphous silicon film 17a is deposited on the whole **insulating layer** 14 with the connecting **hole** 15 formed therein, Subsequently, a tantalum **oxide film** 17c is formed on the silicon film 17a by thermal decomposition method. As a result, a **silicon oxide film** 17b is formed in the interface between the silicon **film** 17a and tantalum **oxide film** 17c. Thus, the uniformity at the time of dielectric breakdown of a thin **insulating film** formed on a metal can be improved remarkably.

7/3,AB/38 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04638704
SEMICONDUCTOR DEVICE

PUB. NO.: 06-310604 [JP 6310604 A]
PUBLISHED: November 04, 1994 (19941104)
INVENTOR(s): JINRIKI HIROSHI

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APPLICANT(s): KAWASAKI STEEL CORP [000125] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-092961 [JP 9392961]
FILED: April 20, 1993 (19930420)

ABSTRACT

PURPOSE: To provide **antifuses** whose insulation is destroyed by write voltage uniformly, and to raise the reliability of semiconductors having these **antifuses**.

CONSTITUTION: This semiconductor device has a plurality of **antifuses** composed of an **insulating layer** 24 formed between a first metal wiring 21 and a second metal wiring 23, connecting **holes** 25 formed in this **insulating layer** 24, and an **insulating film** 27 formed in these connecting **holes** 25 to insulate between the first metal wiring 21 and the second metal wiring 23. The **insulating film** 27 is composed of **Ge** (sub 10)Te(sub 50)As(sub 30) being material which changes its phase by the application of write voltage and becomes conductive. When the write voltage is applied between the first metal wiring 21 and the second metal wiring 23, an amorphous **insulating film** 27 to which voltage is applied crystalizes, and crystals J are produced. These crystals J are conductive, and the first metal wiring 21 and the second metal wiring 23 are connected by them.

27/3,AB/39 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

04630801
SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

PUB. NO.: 06-302701 [JP 6302701 A]
PUBLISHED: October 28, 1994 (19941028)
INVENTOR(s): JINRIKI HIROSHI
KAIZUKA KENJI
OOTA TOMOHIRO
APPLICANT(s): KAWASAKI STEEL CORP [000125] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-090319 [JP 9390319]
FILED: April 19, 1993 (19930419)
JOURNAL: Section: , Section No. FFFFFF, Vol. 94, No. 10, Pg. FFFFFF, FF, FFFF (FFFFFFFF)

ABSTRACT

PURPOSE: To enhance the reliability of **antifuse** by forming a **dielectric film** and a conductive path or the like between first and second metal wirings and then applying a voltage therebetween thereby breaking the **dielectric film** and conducting the first and second metal wirings.

CONSTITUTION: An **antifuse** is formed between first and second metal wirings 21, 27. A conductive path 23 is composed of tungsten and formed by making a contact **hole** 29 by boring a **dielectric layer** 24, applying tungsten by CVD, and then filling the contact **hole** by etch back. The second metal wiring 27 is patterned onto the **dielectric**

film 25 using TiN/aluminium and a passivation film 28 of PSG/plasma **silicon nitride** is formed as a protective film. Since the conductive path 23 is embedded, the **dielectric film** 25 can be made thin and flattened. Consequently, the **dielectric film** 25 can be uniformly broken down dielectrically even when low writing voltage is employed thus conducting the first and second metal wirings 21, 27.

27/3,AB/40 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04129852
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 05-121552 [JP 5121552 A]
PUBLISHED: May 18, 1993 (19930518)
INVENTOR(s): FUJIWARA YUKIO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-278013 [JP 91278013]
FILED: October 24, 1991 (19911024)
JOURNAL: Section: E, Section No. 1426, Vol. 17, No. 484, Pg. 51, September 02, 1993 (19930902)

ABSTRACT

PURPOSE: To provide a method for improving yield of **antifuse** by reducing occurrence of defect in an amorphous silicon layer by irradiating it with inert gas ions removing a surface product to be executed before an upper layer interconnection is formed and stabilizing phase transition characteristics.

CONSTITUTION: A lower wiring layer 3 is formed on a substrate 1, an interlayer **insulating film** 4 is formed thereon, patterned, and removed from above the wiring 3 to from contact **holes** 5.51 Then, an amorphous silicon layer 6 is formed in the **hole** 5 of an **antifuse** forming region, the surface of the layer 6 is oxidized to from a **silicon oxide film** 8, a surface product 7 in the **hole** 5 of a region except the **antifuse** forming region and the film 8 are removed by irradiating it with inert gas ions, and an upper wiring layer 9 is formed on the film 4 including the **holes** 5.51.

27/3,AB/41 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

03178052
SEMICONDUCTOR ELEMENT AND ITS MANUFACTURE

PUB. NO.: 02-153552 [JP 2153552 A]
PUBLISHED: June 13, 1990 (19900613)
INVENTOR(s): NAKASAKI YASUTAKA
HIRAKAWA KAZUYOSHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-124486 [JP 89124486]
FILED: May 19, 1989 (19890519)
JOURNAL: Section: E, Section No. 972, Vol. 14, No. 408, Pg. 68, September 04, 1990 (19900904)

ABSTRACT

PURPOSE: To obtain a programmable element having a high OFF resistance and a low ON resistance by using a semiconductor element having electrodes as **anti-fuses** over or under which amorphous silicon and **insulating** silicon **films** are provided.

CONSTITUTION: An N(sup +) layer (a lower electrode) is provided in an Si substrate 101, a **hole** is opened in an interlayer **insulating film** 103, an **SiO**(sub 2) film 107 and an amorphous Si film 105 are superposed in the **hole** in the order of the films 107 and 105 by a CVD method and an upper electrode 106 is formed on the patterned amorphous Si film 105 and is used as an electrode of a three-layer structure. Another electrode is provided in a **hole** provided at the time of a second patterning. By the three-layer structure, the OFF resistance of an element is secured by the **SiO**(sub 2) film of a high specific resistance and the reliability of an **anti-fuse** of the element is secured by the characteristics of the amorphous Si film. The OFF resistance can be easily broken down by a program voltage by making thin the **SiO**(sub 2) film and can be brought into a low resistance state without having an effect on the ON resistance of the element.

/3,AB/42 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

03171245
SEMICONDUCTOR ELEMENT AND MANUFACTURE THEREOF

PUB. NO.: 02-146745 [JP 2146745 A]
PUBLISHED: June 05, 1990 (19900605)
INVENTOR(s): NAKASAKI YASUTAKA
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-185387 [JP 89185387]
FILED: July 18, 1989 (19890718)
JOURNAL: Section: E, Section No. 969, Vol. 14, No. 394, Pg. 15, August 24, 1990 (19900824)

ABSTRACT

PURPOSE: To secure R(sub off) which is equivalent to an **insulating material** as amorphous silicon and utilize effect of reduction in R(sub on) due to inclusion of impurities ion by forming a semiconductor element constituting an **antifuse** in four-layer structure of a lower-part electrode, amorphous silicon, a silicon **insulation film**, and an upper-part electrode.

CONSTITUTION: A semiconductor which allows the area between one electrode 104 and the other electrode 106 to change from high-resistance state to low- resistance state by applying voltage between the electrodes 104 and 106 formed on the surface of a semiconductor substrate 101 for making a current flow is in four-layer structure consisting of the upper-part electrode 106, an amorphous silicon 105, a **silicon oxide insulation film** 107, and a lower-part electrode 102. For example, the impurities diffusion layer 102 is formed at the Si semiconductor device 101 and an interlayer **insulation film** 103 is formed over the entire surface, and then a contact **hole** 108 is formed. Then, **SiO**(sub 2) is accumulated by 100 angstroms or less and the amorphous silicon 105 is formed on it for patterning. Then, an interlayer **insulation film** 103a is accumulated over the entire

surface and contact **holes** 108a and 109 are formed, and then the wiring electrode 104 and the upper-part electrode 106 are formed.